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Service Manual

SERVICE GUIDE

ORDER NO.
ARP 1702

CD CDV LD PLAYER

CLD-3070

CONTENTS

1. DESCRIPTION OF BOTH-SIDES PLAYBACK MECHANISM (α-TURN SYSTEM)

1-1 OUTLINE

The both-sides playback mechanism is called "α-Turn System" and has the following features:

- The signal reading by the pickup ass'y from the disc surface is performed in the same way when playing both sides A and B.
- The relationship of the three beams (zero and first order beams) for signal read-out is the same when playing both sides A and B.
- The direction of rotation of the spindle motor is reversed when playing side B.

1-2 OUTLINE OF OPERATION

Fig. 1-1-1 shows the operating principles of the system.

The carriage assembly for side-A play moves toward the inner or outer edge of the disc guided by the carriage shaft (A). When the Carriage Assembly is inverted from Side A to Side B, the carriage assembly is moved toward the outer edge of the disc, through the carriage shaft (A) to the guide shaft at the inversion mechanism, and at the same time, the inversion mechanism starts rotating. At the position where the inversion mechanism is rotated by 180°, the carriage assembly is fed toward the inner edge of the disc, and passed by the guide of the guide shaft to the carriage shaft (B) then the carriage assembly is moved toward the inner edge of the disc to start playing side B.

Changing from sides B to A is performed in the opposite way.

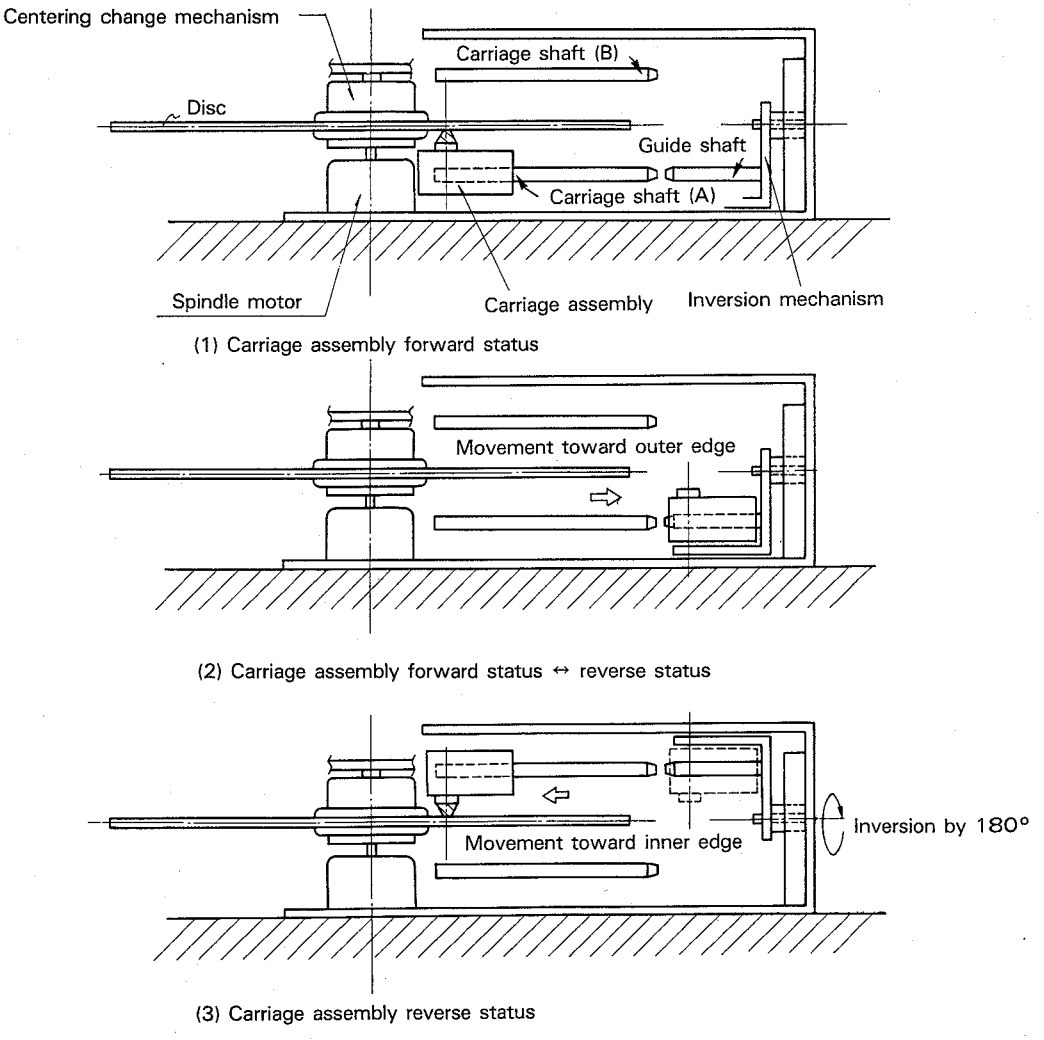


Fig. 1-1-1 Operating principle of "both-sides playback mechanism" (α-turn system)

Fig. 1-1-2 is a diagram showing the outline of the "α-turn" system both-sides playback mechanism. In this system, since the two carriage shafts (A) and (B) are securely fixed along the upper and lower surfaces of the disc, while the guide shaft in the inversion mechanism is located on the same axis with respect to each carriage shaft (A) and (B) when playing both sides A and B, the transition of the carriage assembly can be performed smoothly.

The pickup assembly is located inside the carriage assembly, in which the slider drive mechanism used for the movement of the pickup assembly (it is also used for driving the turn-gear to invert the carriage assembly), tilt drive mechanism and height drive mechanism (described below) are also incorporated.

The above inversion operation is started when the turn gear located at the rear of the carriage section is engaged with the internal gear (sun gear). Then the entire carriage section is turned by 180° by means of the rotation of the turn gear (planetary gear). In this system, the invertion mechanism itself does not have an exclusive drive section.

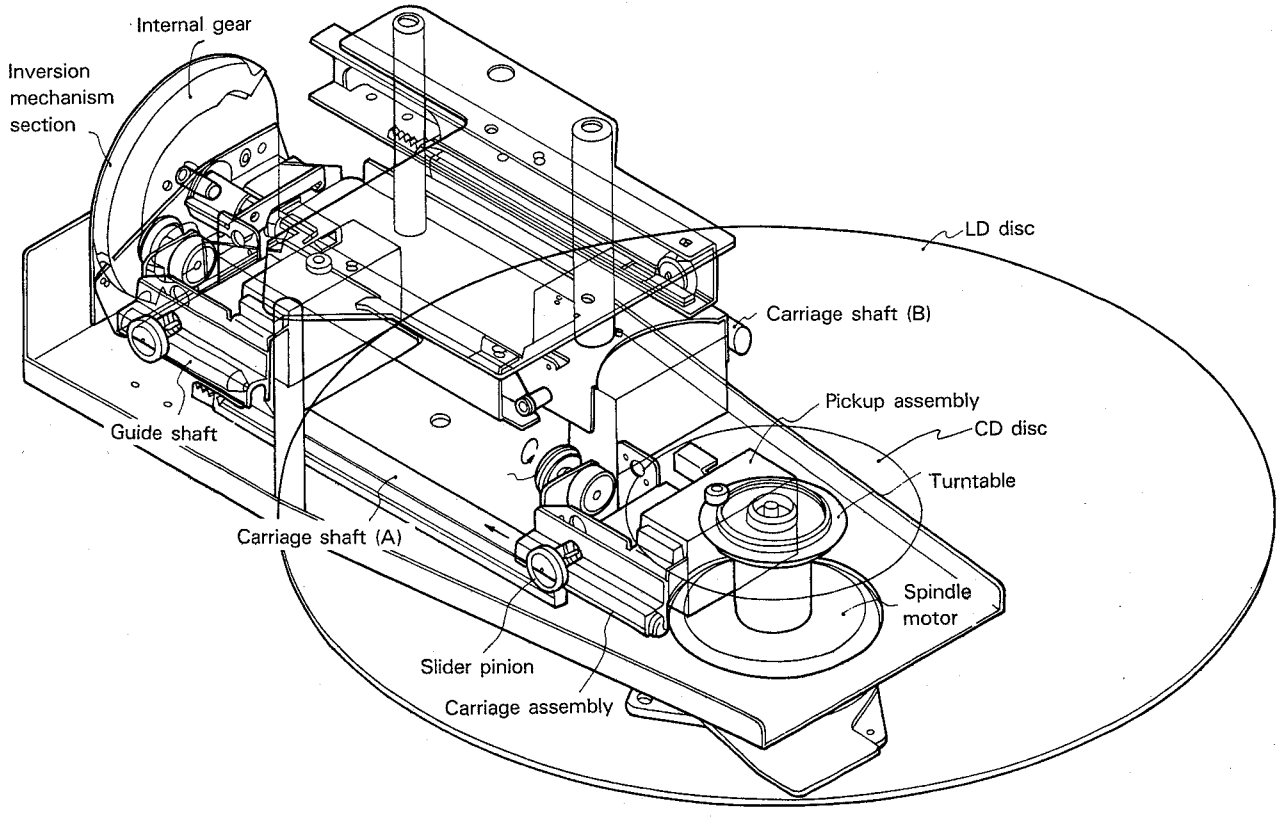


Fig. 1-1-2 Overall diagram of the "Alpha-Turn" both-sides playback mechanism

2. DESCRIPTION OF CLAMPER MECHANISM

2-1. OUTLINE

Eccentricity due to errors when the two sides of the disc are attached may increase time base errors and cause Color Band. Therefore, the centering ability of the clamper mechanism is especially important in a both-sides playback system.

Because of this, the CLD-3070 is equipped with a clamper mechanism having an independent centering system for sides A and B and side B of the disc can be played back with the same stability as side A.

2-2 OUTLINE OF OPERATION

In the side A/B independent centering system, the centering hub (B) is pointed inside the disc clamper. Fig. 2-2-1 shows its structure and the operation. In status (2) when side A is clamped, in the same way as in the conventional system, the center of side A is adjusted to the center of the spindle motor by applying the tapered section of the centering hub (A) to the inside of the center hole on side A of the disc and the disc is clamped to the turntable by the disc clamper.

When playing side B from this condition, the clamper holder which maintains the clamper mechanism is lowered to lower the centering hub (B) located inside the disc clamper. Then, while the centering hub (A) is lowered, the tapered section of the centering hub (B) comes into contact with the inner edge of the center hole on side B of the disc in which there is a displacement between sides A and B. When the clamper holder is further lowered, the centering hub (A) is completely released from the disc while the disc is pressed by the tapered section of centering hub (B). So that this is possible, the disc is held at the center of the spindle motor while it is shifted to the surface of the turntable, then the mechanism goes to status (3).

As described above, the side A/B independent centering mechanism is constructed simply by furnishing the independent centering hubs (A) and (B) and provides the same centering accuracy as the conventional system.

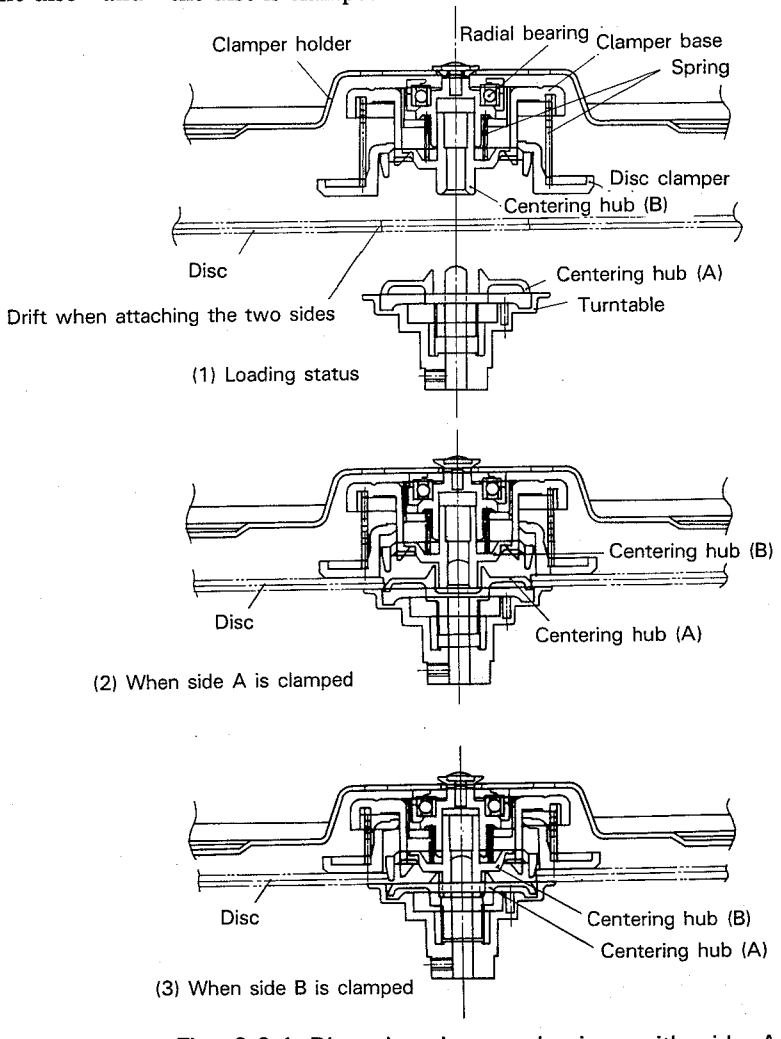


Fig. 2-2-1 Disc clamping mechanism with side A/B independent centering system

3. TILT & HEIGHT SERVO MECHANISM

3-1 OUTLINE OF OPERATION

Fig. 3-1-1 shows a comparison between the conventional tilt mechanism and the newly developed Tilt & Height Mechanism.

Fig. 3-1-2 shows the structure of the Tilt & Height Mechanism.

In this system, since the tilt fulcrum is located on the extension of the center line of the beam axis of the pickup, the light axis angle can be swung by the exclusive tilt drive mechanism. And since this tilt fulcrum is supported by the AF arm, it can also be moved up/down by swinging the AF arm with the exclusive height drive mechanism. The tilt servo is controlled by the output of the tilt sensor which detects the angle of the warpage of the disc so that the laser beam is always emitted at right angles to the disc. The height servo mechanism controls it so that the operating distance (the optimum distance for the focus servo) of the pickup above the disc is always kept at a fixed value.

With the above method, since the angle and displacement can be compensated independently, there will be no residual tilt error with uneven or warped discs while discs are played back with optimum focus servo. Therefore, the optimum pickup performance will be obtained and the playing ability will be greatly improved.

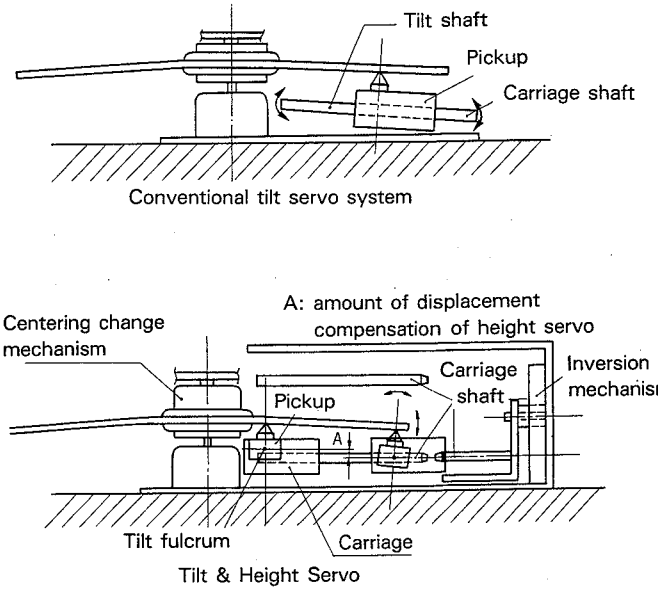


Fig. 3-1-1 Comparison between the conventional tilt servo and the "tilt & height servo"

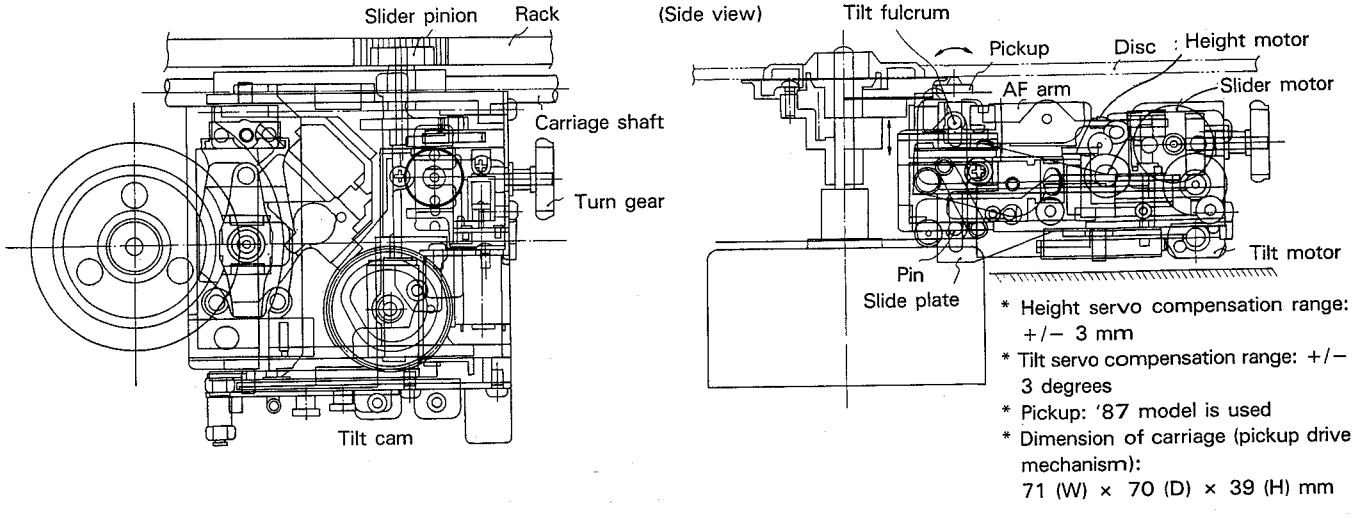


Fig. 3-1-2 Structure of pickup drive mechanism used in both-sides CLD player

3-2 DESCRIPTION OF HEIGHT SERVO

The focus lens focuses the laser beam on the pit surface of the disc to read out the recorded signal. If a warped disc is loaded, normally the lens is moved up and down slightly to position the fulcrum center of the stroke. When the inner area of the disc is being played back, and is moved much more due to the warping of the disc when the outer area is being played back. Therefore, the dynamic range of the lens may become uneven for the top and bottom sides.

To compensate for this, in the conventional system, the slidershaft is rotated while it is swung up and down using the point where the shaft is located as a supporting point to assure the dynamic range of the lens. (Fig. 3-2-1)

As opposed to this, in the Tilt & Height Servo Mechanism, the entire pickup assembly is moved up and down.

The DC component of the current flowing in the focus lens is proportional to the distance from the pickup body (l_2). To operate, this current is converted into voltage E_R by the resistor R_1 and this is used to move the entire pickup assembly up and down by rotating the motor when E_R exceeds a positive or negative fixed value (E_{TH}), so that the focus lens is used within its effective stroke. Fixed value E_{TH} is set at 1/4 of the stroke between the upper and lower limits, considering the operating sensitivity of the lens. (Fig 3-2-2)

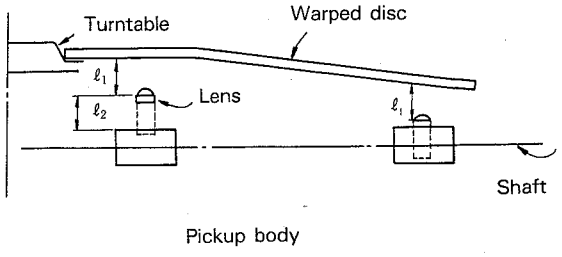


Fig. 3-2-1

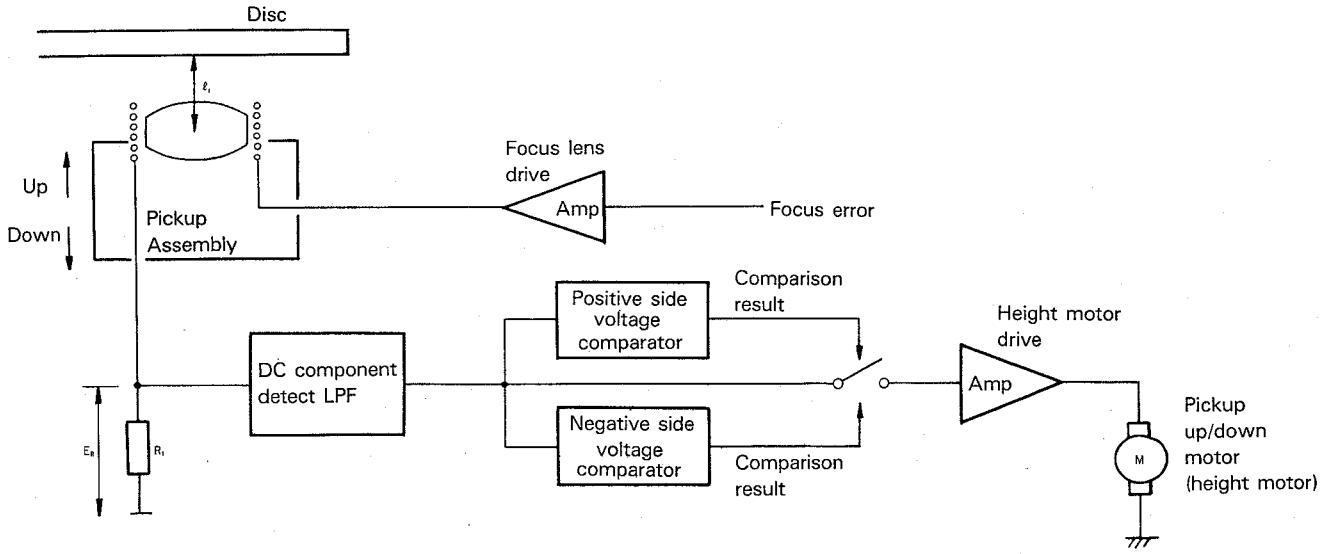
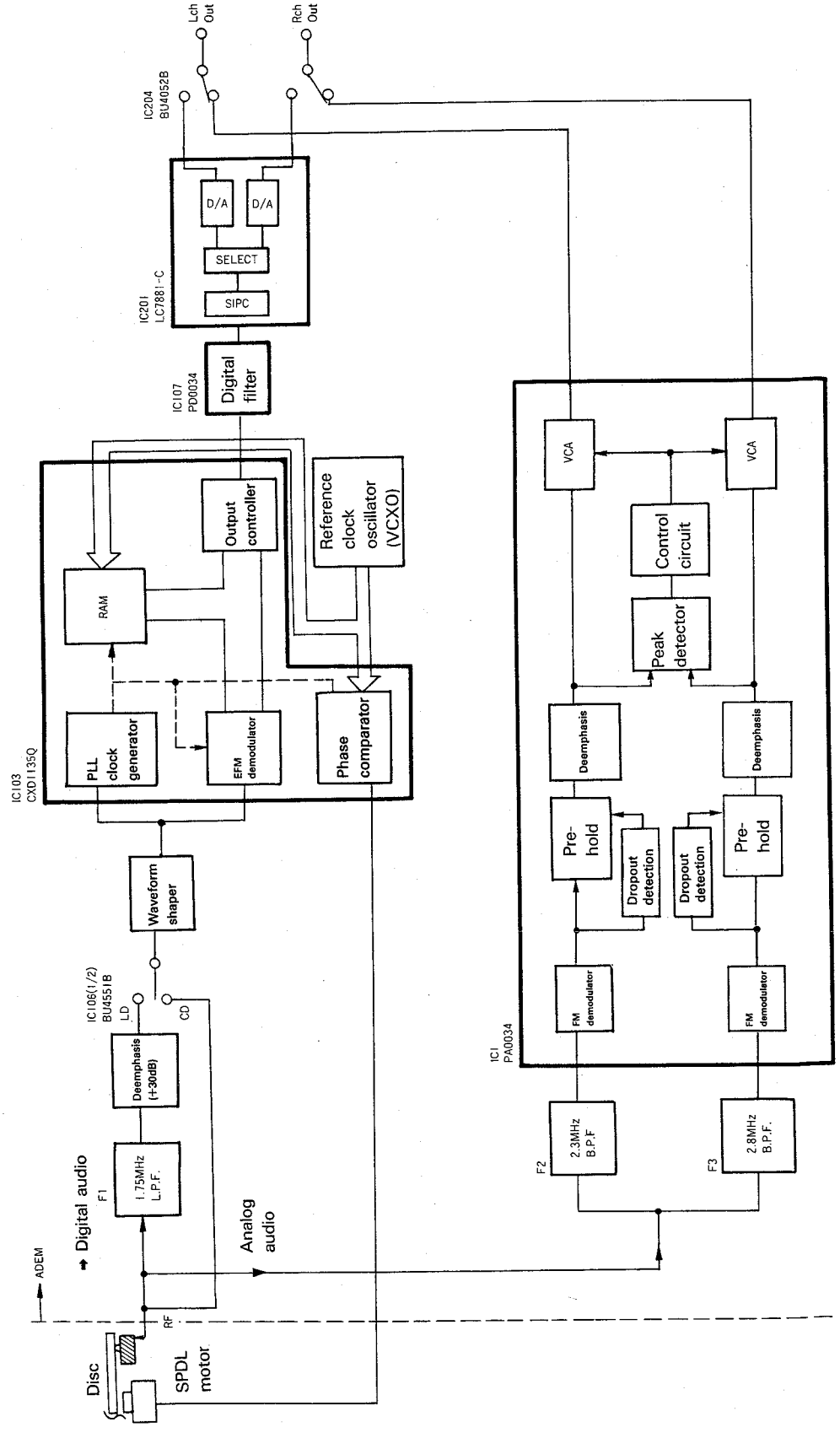


Fig. 3-2-2 Height servo block diagram

4. AUDIO SIGNAL PROCESSING CIRCUIT



Audio Signal Processing Circuit Block Diagram

4-1 OUTLINE

The ADEM assembly accepts the RF signal from the VSOP assembly and performs the required audio signal processing. The main IC in the analog audio circuit is PA0034 (Audio Demodulation & CX Demodulation), while the main IC in the digital audio circuit is CXD1135Q.

4-2 DESCRIPTION OF PA0034

After the FM audio signal from the band-pass filters (2.3 MHz for L-channel and 2.8 MHz for R-channel) is demodulated, the resultant signal is passed through the pre-hold circuit, deemphasis circuit and VCA (voltage controlled amplifier), and is then output as the analog audio signal.

If dropout occurs, it is detected by the dropout detector. When dropout is detected, the signal level is maintained at the value immediately before the dropout occurs by the pre-hold circuit, to prevent noise from occurring. Further, CX noise reduction is provided to improve the audio dynamic range as well as the signal-to-noise ratio.

PA0034 is a one-chip IC exclusively for LD audio, and performs the whole of the above signal processing. Fig. 4-2-1 shows the functions of each pin, while the internal block diagram is shown in FIg. 4-2-2.

4-3 DESCRIPTION OF CXD1135Q

CXD1135Q has the following function

1. Generation of the bit clock (PLCK: 4.3218M) by EFM-PLL
2. EFM signal demodulation, error correction and interpolation
3. Frame synch. signal detection, protection and interpolation
4. Subcode signal demodulation and error detection
5. SPDL servo (obligatory deceleration/acceleration, brake, speed servo, phase servo)
6. Zero cross counter for 8-bit tracking error (not found in these models)
7. Double oversampling digital filter (35-stage)
8. Digital audio interphase output

The pin connection diagram of CXD1135Q and its internal block diagram are shown in Fig. 4-3-1.

Item No.	Symbol	Function	Item No.	Symbol	Function
1	VEER	Power supply pin	22	LOUT	L-ch output
2	VINR	FM signal input	23	STC2	STC pin 2
3	BIASR	Input bias	24	STC1	STC pin 1
4	VREFR	Internal reference power supply	25	VCC	Power supply pin
5	GNDR	Ground pin	26	COMP	Compensator pin
6	ALCR	ALC capacitor pin	27	TBC	TBC error signal input pin
7	CSR	Carrier removal pin	28	CINL	CX control signal input
8	DOS2R	DOS2 input	29	CXINL	CX input
9	DEMOR	Demodulator output	30	SWOL	Mode select amp output
10	SINR	Dropout compensator switch input	31	SWINL	Mode select amp input
11	DOCR	Dropout compensator switch output	32	DOCL	Dropout compensator switch output
12	SWINR	Mode select amp input	33	SINL	Dropout compensator switch input
13	SWOR	Mode select amp output	34	DEMOL	Demodulator output
14	CXINR	CX input	35	DOS2L	DOS2 input
15	CINR	CX control signal input	36	CSL	Carrier removal pin
16	R	Mode select pin R	37	ALCL	ALC capacitor pin
17	L	Model select pin L	38	GNDL	Ground pin
18	CX	CX control	39	VREFL	Internal reference power supply
19	FTC	For connection of FTC capacitor	40	BIASL	Input bias
20	GNDCX	Ground pin	41	VINL	FM signal input
21	ROUT	R-ch output	42	VEEL	Power supply pin

Fig. 4-2-1 PA0034 pin functions

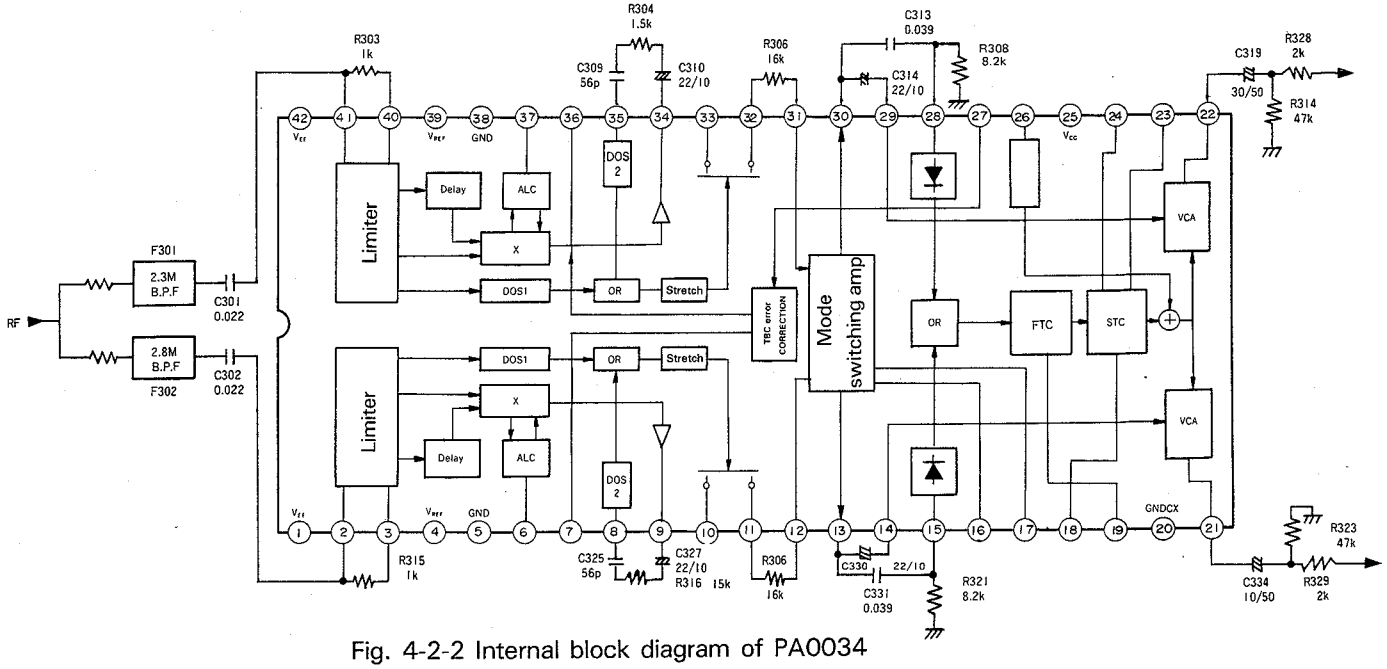


Fig. 4-2-2 Internal block diagram of PA0034

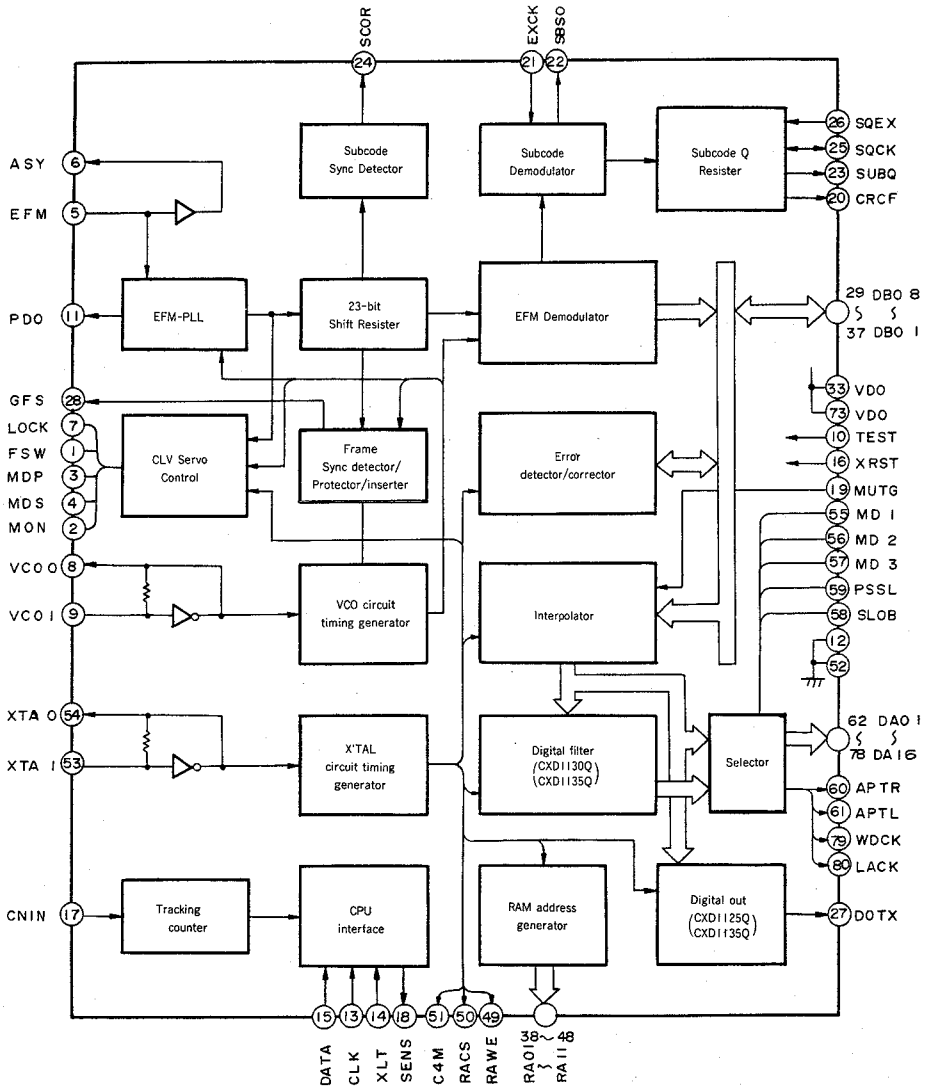


Fig. 4.3.1 Internal block diagram of CXD1135Q

4-4 CXD1135Q COMMAND CODE

As the table below shows, CXD1135Q has a 4-bit register containing addresses 9 through E. Player operations can be performed by sending 8-bit data (command code) containing address and data (totalling 8-bits) to these addresses.

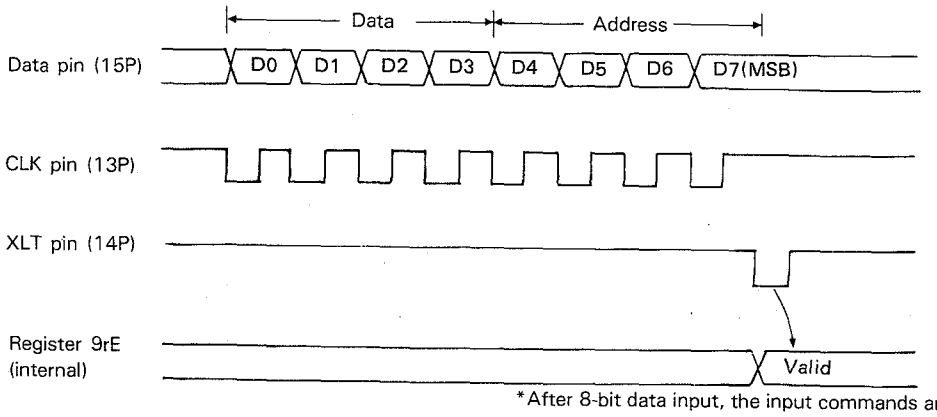
*Note: FOR STATUS
H: High Level
L: Low Level
Hi-Z or Z: High impedance
P: Pin No. of IC

<Register Chart>

Register Name	Command	Addresses D7 – D4	Data				SENS pin (18P)
			D3	D2	D1	D0	
9	Control of new functions	1001	ZCMT	HZPD	NCLV	CRCQ	Z
A	Synch protection, attenuation control	1010	GSEM	GSEL	WSEL	ATTM	Z
B	Counter set, Lower 4-bits	1011	Tc3	Tc2	Tc1	Tc0	COMPLETE
C	Counter set, Upper 4-bits	1100	Tc7	Tc6	Tc5	Tc4	COUNT
D	CLV control	1101	DIV	Tz	Tp	GAIN	Z
E	CLV mode	1100		CLV mode			Pw≧64

* The B.C register is for tracking error zero cross count and is not employed in the 1988 models.

<Data Input Timing Chart>



*After 8-bit data input, the input commands are executed during the time period when XLT is L. Data input timing is the same as in the CXA1082A.

«Information about the Registers»

- **Register 9**

		Dn=0	Dn=1
ZCMT	D3	Zero cross MUTE OFF	Zero cross MUTE ON
HZPD	D2	The PDO pin is always active	The PDO pin is Z at the trailing edge of GFS
NCLV	D1	CLV-P servo supported by frame synch signal	CLV-P servo supported by base count
CRCQ	D0	CRCF is not superimposed on SUBQ	At the leading edge of SCOR, SUBQ= CRCF
		(Functions identical to those of the CX23035)	(New functions)

ZCMT: Turns zero cross MUTE ON/OFF.
HZPD: Switches PD output to Hi-Z (ON/OFF) from the trailing edge of the GFS pulse (GFS is H when SPDL LOCK is activated) to a maximum of 0.55nS. (PLCK and play EFM undergo phase comparison, and the PD output controls the VCO.)
NCLV: Switches the SPDL phase servo error detection method when PLL is locked.
CRCQ: Switches the output of CRCF data from the subcode data Qoutput pin, SUBQ, ON/OFF.

If the content of Register 9 is cancelled out by activating POWER ON RESET and none of its commands are active, the IC will function exactly like the CX23035.

• **Register A**

Controls the 4 signals: GSEM, GSEL, WSEL, ATTM.

GSEM	GSEL	Frame
0	0	2
0	1	4
1	0	8
1	1	13

When frame synch detection is not working properly, a dummy frame synch is interpolated, but the number of frames for which interpolation will be performed is fixed: during LD play, 8 frames; during CD play 8 frames; and during SCAN, 13 frames.

WSEL	Clock
0	±3
1	±7

To prevent errors during frame synch detection, a detection window of a certain width is set and synch patterns which fall outside the detection window are ignored.

The width of the detection window is set as follows: (set at ±7 clock)

ATTM	MUTG pin	dB
0	0	0
0	1	−∞
1	0	−12
1	1	−12

In combination with the MUTG pin (19P), MUTE ON/OFF and the application of -12dB attenuation can be controlled.

In terms of actual command code, $AA is being input. Since A = 1010 and GSEL = 1, GSEL = 0, there are 8 interpolation frames with detection width parameter set at 7 clock.

• **Register D**

DIV	D3	0	RFCK/4 and WFCK/4	Phase comparison frequency in CLV-P mode
		1	RFCK/8 and WFCK/8	
TB	D2	0	RFCK/32	Bottom hold cycles in CLV-S, CLV-H modes
		1	RFCK/16	
TP	D1	0	RFCK/4	Peak hold cycle in CLV-S mode
		0	RFCK/2	
GAIN	D0	0	−12dB	MDP pin gain in CLV-S, CLV-H modes
		1	0dB	

RFCK: Read Frame Clock (frequency divided from X'TAL, 7.35k)

WFCK: Write Frame Clock (Frame synch during play EFM)

CLV-P mode: Phase servo which operates when the PLL loop is locked

CLV-S mode: Speed servo which operates when the PLL loop is not locked

CLV-H mode: Speed servo during search (when pickup is moving)

In terms of actual command code, $D4 is being input. Since 4 = 0100, RFCK, WFCK are frequency divided by 4 for phase error, RFCK is frequency divided by 16 for bottom hold in the CLV-S mode, RFCK is frequency divided by 4 for peak hold and MDP pin gain is −12dB.

• **Register E**

		(3P)	(4P)	(1P)	(2P)
Mode	D3–D0	MDP pin	MDS pin	FSW pin	MON pin
STOP	1000	L	Z	L	L
KICK	1000	H	Z	L	H
BRAKE	1010	L	Z	L	H
CLV-S	1110	CLV-S	Z	L	H
CLV-H	1100	CLV-H	Z	L	H
CLV-P	1111	CLV-P	Z	L	H
CLV-A	0110	CLV-S or CLV-P	Z or CLV-P	L or Z'	H
CLV-A'	0101	CLV-S' or CLV-P	Z or CLV-P	L or Z	H

This register sets the operating mode for the SPDL servo. In this mode, the SENS pin, 19P, registers L when the frame sync pulse amplitude detected at CLV-S is over 64T. This output, however, is not utilized.

From commands 0000 to 0110, the system is identical to that of the CX23035.

After the focus servo lock check, actual SPDL start is performed by $E8, i.e., command code 1000 puts the unit into KICK mode which force starts the SPDL. Next, $E6 puts the unit into CLV-A mode which closes the SPDL servo and PLL loop. The lock can be checked by verifying that GFS registers an H.

When stopping, $EA, command code 1010, applies the brake, and after SPDL stop detection at FG, $EO puts the unit into stop mode. Because the CLD-3070 has a 4-times oversampling digital filter IC (PD0034), the digital filter in the CXD1135Q is not utilized.

As a digital OUT terminal, the toss link for optical fiber transmission is passed through a buffer and connected to 27P. However, since the function assigned to MODE 0 of the digital OUT IC, 27P is no longer needed for this purpose. Instead, modulated output for the digital audio interface format is obtained from 27P.

ON/OFF for digital filter and OUT functions can be fixed according to the H and L signals from MD1, 2 and 3 of 55, 56 and 57P. On the CLD-3070 these are set at L, L, H corresponding to digital, OFF and digital OUT, ON.

4-5 SIGNAL PROCESSING AND CXD1135Q PERIPHERAL CIRCUITRY

The EFM signal passes through the ATC circuit made up of IC101 (BU74HCU04) and IC108 (2/2) (NJM082D) and is input to IC103 — 5P (CXD1135Q). The result of phase comparison between EFM and the VCO output of IC108 (1/2) is output from IC103 — 11P and controls the VCO. These compose a PLL loop.

IC103 performs SPDL servo error detection from EFM and the output of 1 through 4P is utilized for the SPDL servo. The function of the pins is as follows:

FSW (1P): When the PLL loop is locked, it is Hi-Z. At other times it is L.
IC105 (1/2) (NJM082S) is the phase and speed error mix filter, and is used to switch the cut-off frequency. (Hi-Z, 500Hz, L: 20Hz).

MON (2P): When the motor is stopped: L, when rotating: H.

MDP (3P): SPDL phase error when PLL is locked and otherwise, speed error

MDS (4P): Speed error when PLL is locked and, otherwise, Hi-Z

Internal detection of whether PLL is locked or not, is performed at the GFS pin, 28P, which registers H when PLL is locked.

During CD or the audio section of a CDV play, the error signal of IC105 — 8P is input as CD ERR to the absolute value amp for the SPDL servo section from IC106 — 5P (BU4551B) and drives the SPDL motor.

During LDD play or the video section of a CDV, error signal is output from IC106 — 5P to control IC108 VCXO. As a clock signal, VCXO output signal is input to IC103 — 8P. At IC103 the demodulated digital audio data is input as serial data to IC107 (PD0034) along with 80P LRCK (44.1k) and 76P C210 (2.1168M).

IC107 is a 4-times oversampling digital filter.

The CLD-3070 utilizes a sub-CPU, IC102 (PDE024), to handle the transmission of 8-bit serial command data to IC103 (CXD1135Q) and the reception of sub-code data from IC103.

IC102 is connected to the main CPU by the 4-bit data bus and by the signal lines ATN, STB and ACK.

However, with the introduction of TOC (ADR = 4) in LDD discs, the reading of the TOC renders processing time too long and it is no longer practical for the main CPU to directly read the data.

For this reason, sub-code data from CXD1135Q is placed in a buffer at IC102 (PDE024) and, in response to a command from the main CPU, is transmitted by 4-bit bus. In addition, command code destined for CXD1135Q is input through IC102.

On the basis of data received from CXD1135Q and the main CPU, IC102 performs digital/analog switching, LD/CD switching and Emphasis ON/OFF.

Another function of IC102 is to output LSEL and RSEL signals used for switching Left/Right channels during LDD play:

	Both CH	RCH only	LCH only
LSEL	L	L	H
RSEL	L	H	L

5. VIDEO SIGNAL PROCESSING SYSTEM

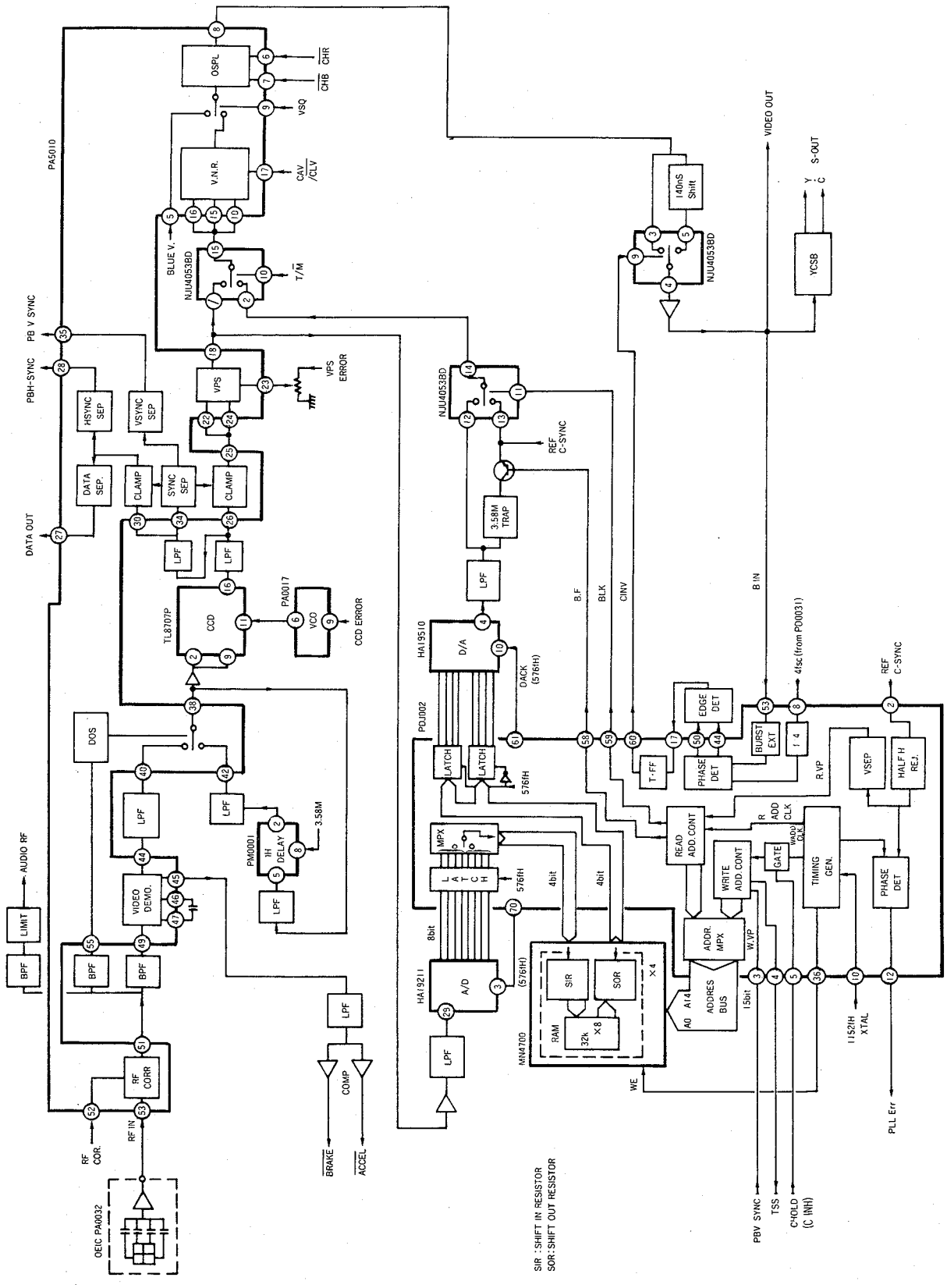


Fig. 5-1 Video signal processing system block diagram

5.1. OUTLINE

The pickup of this model incorporates a unitized IC (PA0032) containing both photodetectors and head amp section. After gain adjustments have been made on the FTSB board, the RF output of PA0032 is input to the PA5010 (Video signal processor) of VSOP assembly and is processed.

5.2 DESCRIPTION OF PA5010 (VIDEO SIGNAL PROCESSOR)

PA5010 has the following functions.

- RF signal correction
- Video signal demodulation
- Dropout detection/Video correction SW
- EFM amp
- V-H synch and data separation
- VPS (Video Phase Shifter)
- VNR (Video Noise Reduction)
- Blue background SW and squelch
- Screen display
  (when video memory is OFF or when using blue background screen)

The pin connection diagram of PA5010 and its internal block diagram are shown in Fig. 5-2-1 and Fig. 5-2-2 respectively.

With video that passes through memory, unless the characters (screen display) are inserted before the 140nS (equivalent to one half the cycle of the sub-carrier) shift circuit that is used to maintain sub-carrier continuity between frames (every successive frame undergoes phase inversion). Because only the characters on screen will not be 140nS shifted.

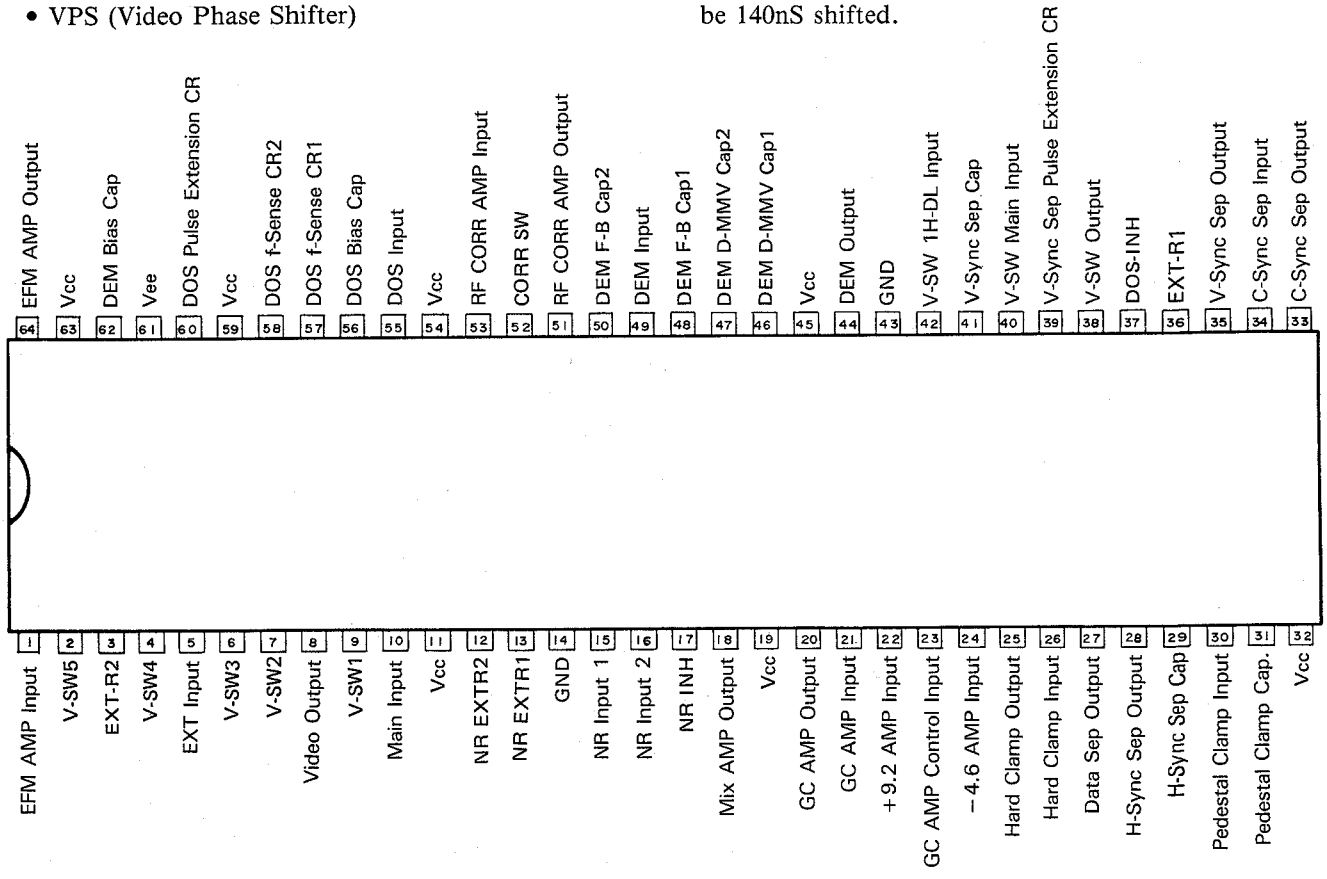
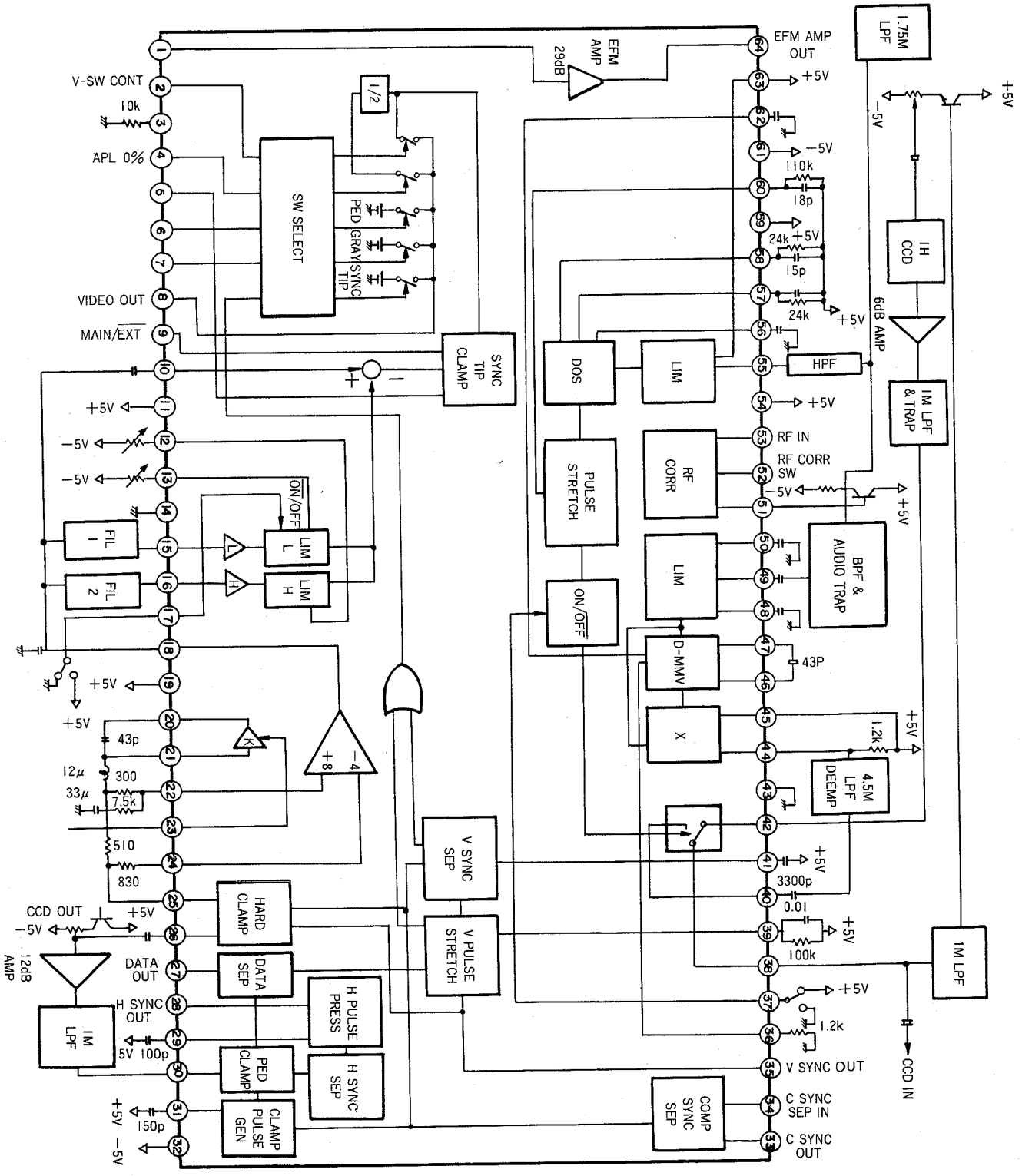


Fig. 5-2-1 PA5010 Pin Connections


EFM AMP OUT
EFM AMP 29dB
1/2
V-SW CONT
10k
APL 0%
SW SELECT
PED
GRAY
SYNC TIP
VIDEO OUT
MAIN/EXT
SYNC TIP CLAMP
+5V
-5V
FIL 1
FIL 2
ON/OFF
LIM L
LIM H
43p
12μ
33μ
300
7.5k
510
830
CCD OUT
12dB AMP
IM LPF
HARD CLAMP
DATA SEP
DATA OUT
H SYNC OUT
5V 100p
H PULSE PRESS
PED CLAMP
H SYNC SEP
CLAMP PULSE GEN
150p
V SYNC SEP
V PULSE STRETCH
DOS
LIM
HPF
PULSE STRETCH
RF CORR
RF IN
RF CORR SW
ON/OFF
D-MMV
X
43P
1.2k
4.5M LPF DEEMP
3300p
0.01
100k
1.2k
V SYNC OUT
COMP SYNC SEP
C SYNC SEP IN
C SYNC OUT
1.75M LPF
IH CCD
6dB AMP
IM LPF & TRAP
110k
18p
24k
15p
BPF & AUDIO TRAP
1M LPF
CCD IN

5.3. SIGNAL PROCESSING IN THE VIDEO MEMORY SECTION

5.3.1. Signal Flow

At the heart of the Video memory section is the 1 M bit D-RAM (MN4700) and RAM control IC (PDJ002). It also includes the A/D (HA19211NT) D/A converter (HA19510).

The IC401 (HA19211NT) is a parallel comparator type A/D converter and the A/D conversion reference voltage has been set at 26P (VRB pin) and 18P (VRT pin). The video signal level is shifted to coincide with the reference voltage, passed through an LPF (low pass filter) and then input to 9P. Reference voltage is 0 and −2V, and signals within that range undergo 8-bits A/D conversion.
The A/D conversion clock signal, which is set at 576fH (=9.06M) is input to IC401 — 3P from IC501 (PDJ002) — 70P.

The 8-bits data is divided at IC401 into an upper and lower 4-bits and transmitted in 4-bits form into memory. 1152fH VCXO is comprised of Q501, Q502 and IC503 (BU74HCU04P) and is controlled at IC503 on the basis of error (output from IC501 — 12P) derived by phase comparison of REF-C-SYNC and memory READ address clock (READ REF-H). If the two signals are not phase locked, REF-C-SYNC insertion position and the D/A converted video signal will not coincide.

Writing to memory is indicated by a WE (WRITE ENABLE) signal from the system controller.

A fixed time difference is maintained between write timing and memory readout timing, and the latter is always performed synchronously with REF-C-SYNC. Furthermore, unless a new frame is written to memory, the previous frame will continue to be output.

The VDEM section of VSOP assembly contains the circuitry that follows D/A conversion. 8-bits data and the 576fH clock signal from IC501 are input to IC505 (HA19510).

If DSPL signal insertion is performed in the VDEM section when memory is ON, dislocation of 140mS occurs between the DSPL display and the memory video due to the fact that the memory video has been passed through the 140nS shift circuit. For this reason DSPL insertion must be performed before 140nS shift.

5.3.2. Necessity of the 140nS Shift

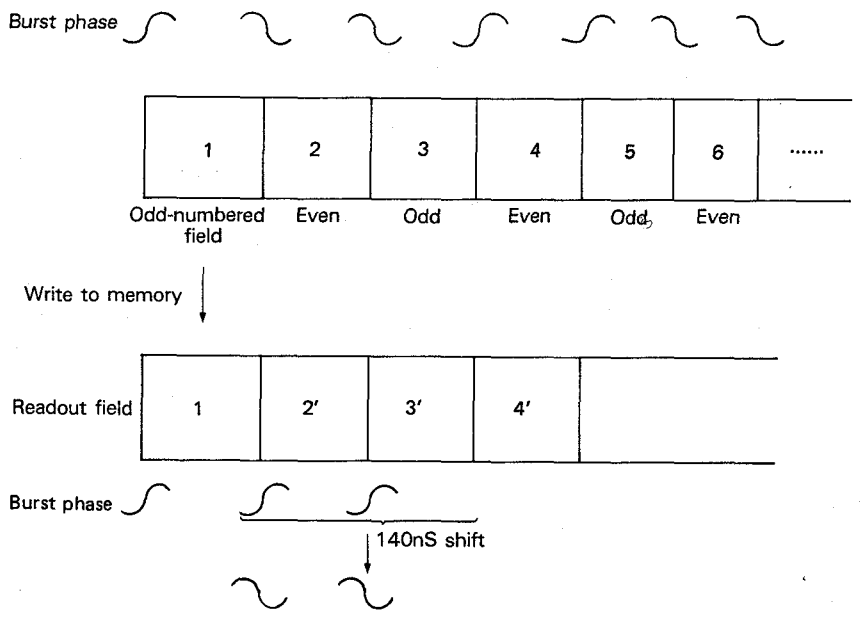
As the figure below shows, the burst phase of the NTSC video signal is reversed for each frame.

If by a still operation as shown below, field No. 1 is written to memory and then continuously read out, the burst phase for every field will become the same. In order to normalize the burst phase, the timing of fields 2' and 3' must be delayed for a period of time equal to one half the periodicity of the burst signal, or 140nS.

By delaying the video signal it is possible to perform an equivalent reversal of burst phase and thereby activate the color lock.

Detection of the discontinuous burst phase is done by comparing the 3.58MHz signal derived by frequency division of the reference clock 4fsc signal input from VSOP at IC501 (PDJ002) of MEM section, with the play burst signal, and then performing edge detection at IC504. The output of edge detection is the C-TRIG signal. This is input to IC501 — 17P and triggers FF in IC501 to output the C-INV signal from 60P which acts as the 140nS shift circuit control signal.

The C-INV signal is then input to IC351 (3/3) — 9P of VDEM section where switching to activate and deactivate 140nS delay is performed.



5.3.3. RAM Control IC (PDJ002)

The CLD-3070 incorporates the PDJ002 as its RAM control IC.

1. V-SYNC separation for REF-C-SYNC, MMV for half H rejection
2. Phase comparator for 4fsc VCXO drive
3. Burst extraction for D/A converted video signal
4. Control signal generation (WRS, CE, RE) for D-RAM (MN4700)
   Address signal generation (A0 — A14) for D-RAM (MN4700)
5. Clock for D-RAM, A/D converter, D/A converter (SCK, LTCK, DACK)
6. Phase comparator to check burst continuity in the D/A converted video signal

5.3.4 Writing Data to RAM

Sampling of the video signal is done at 576fH (=9.06M) with 8-bit quantization.
Data recorded in RAM has 512 samples on the H axis and 256 on the V axis.

$8 \times 256 \times 512 = 1048576$ (bits).

In the CLD-3070, one chip of RAM (MN4700) has the capacity to handle this volume of data.

First of all, the 8-bit parallel data from the A/D converter is divided into an upper and lower 4-bits. Because the D-RAM (MN4700) employed in the CLD-3070 has been specifically designed for video memory applications, it has separate 4-bit data buses for write and readout.

As the figures to the right show, data is sent in 4-bit increments, the upper 4-bits first and then the lower 4-bits, to RAM.

Furthermore, the MN4700 is equipped with an 8-bit serial shift register that can realize 8-bits of information for each bit input to the 4-bit data bus.

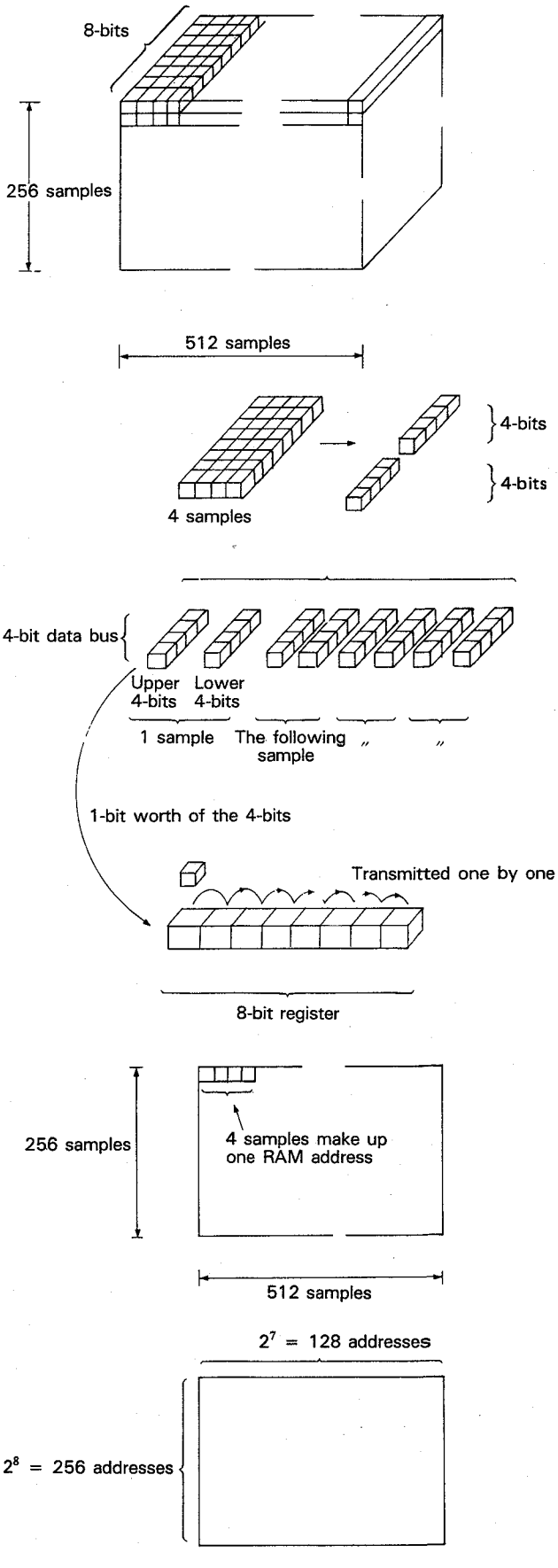
The 8-bit register is transmitted in sequence and when all 8-bits are assembled they are sent to the memory cell to complete recording to memory.

Because 8-bit serial data processing is being employed, one line of the 4-bit data bus, in fact, yields a total of 32-bits. In other words, one block of data handled by the system is equivalent to 4 samples.

In order to arrange and process 4 samples worth of data (=32 bits) in RAM, one RAM address corresponds to 4 samples worth of data. Consequently, the number of RAM addresses required is:

H axis: $512/4 = 128 = 2^7 = 7$-bits
V axis: $256 = 2^8 = 8$-bits
Total bits required = 15-bits.

Because the MN4700 does not employ the address multiplexing normally found in D-RAM which allows switching between row and column addresses, it inputs the addresses as 15bit data.



<Data Processing in RAM>

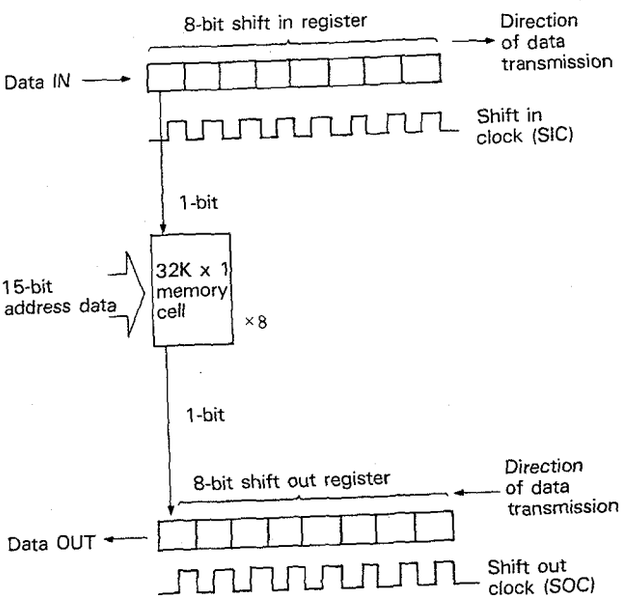
The figure to the right shows one bit worth of data from a 4-bit data bus. Each 8-bit register is connected to a 32K-bit memory cell and in RAM there are a total of 8 × 4 = 32 of these 32K-bit memory cells yielding a memory storage capacity of

32,768 × 32 = 1,048,576.

Because of the need to process the 8-bit data sampled at 576fH in 4-bit units, the frequency of the shift-in, shift-out clock has been set at

576 × 2 = 1152fH (=18.12M).

The necessary clock and timing signals needed for the operation of MN4700, as well as data I/O are all input from the RAM control IC, PDJ002.



6. SPDL SERVO AND TBC (TIME BASE CORRECTOR)

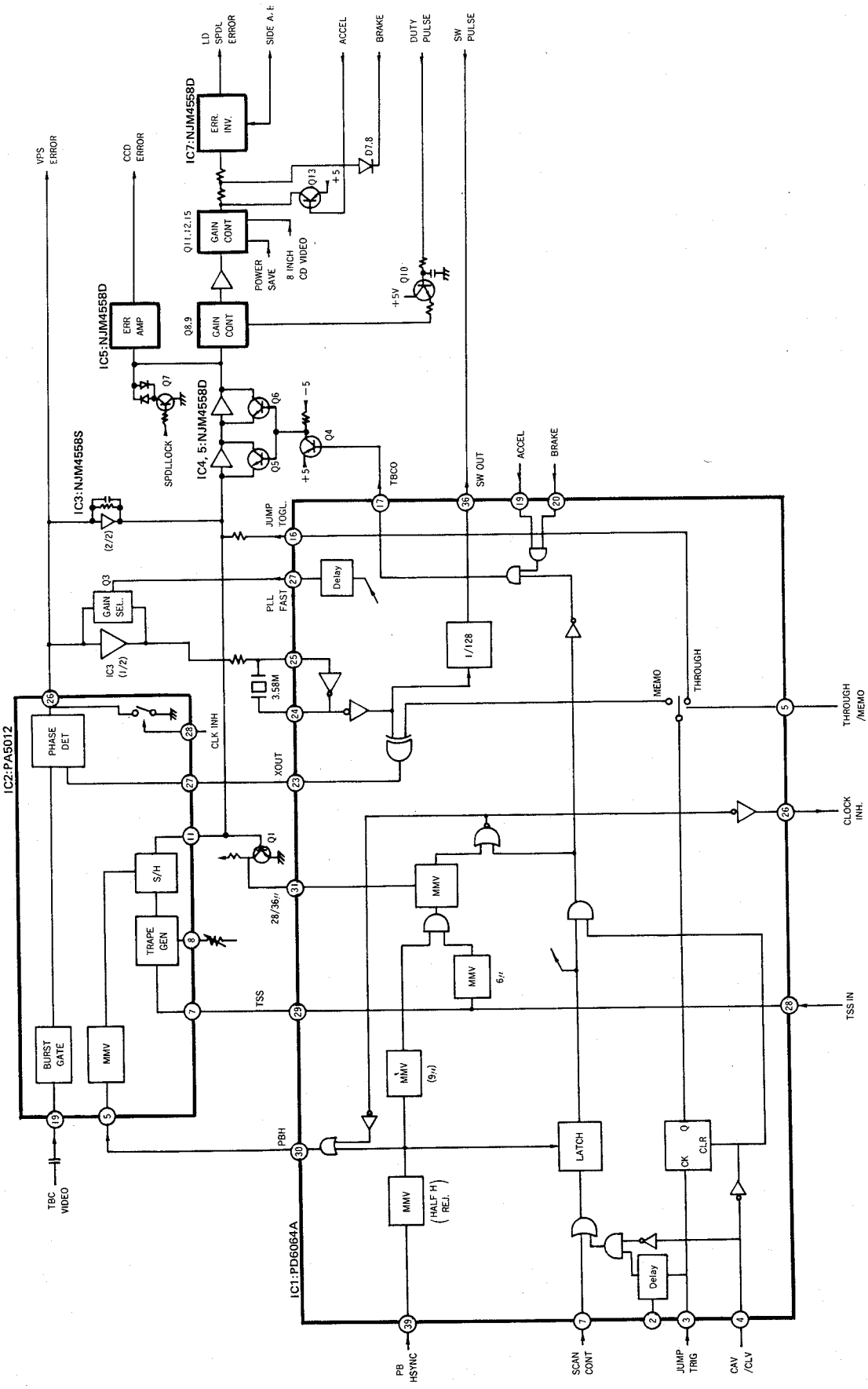


Fig. 6-1 SPDL and TBC block diagram

6.1. DESCRIPTION OF VSOP ASSEMBLY (TBC, CONT) BLOCK DIAGRAM (CLD-3070)

Comparison error between the trapezoid derived from the TSS signal (576fH/576) and PB-H (Playback H-synch) is output by IC2-11P (PA5012) and amplified by error amp IC4 (NJM4558D).

IC5 is the CCD error amp. After the SPDL servo locked, Q7 becomes an error limiter. Q9 and 8 are variable gain amps and, as the collector voltage to Q9 rises, GAIN is lowered.

During CLV disc play, Q10 smooths out the duty pulse which is output by the system microprocessor CPU for SPDL servo loop gain control.

Q11 and 12 are gain switches for 8INCH disc play and CDV disc play, respectively.

- **VPS (Video Phase Shift)**

VPS error is derived by phase shift comparison between PB-B (Playback-Burst) at IC2 and the output of 3.58MHz VCXO near 25 Pin, IC1 — 24 Pin.

Error output from IC2 — 26 Pin is input to the error amp of IC3 (1/2).

Gain switches Q2 and Q3 are for IC3 (1/2). When Q3 is OFF, error detection loop gain increases and activates the FAST mode.

When Q3 is ON, gain is lowered and because the detection loop trails only the low frequency components, high frequency error components remain in the error output of 26 Pin. These are output as VPS error to the VSOP Assembly (VDEM section).

The switch into the FAST mode is performed by means of the PLL FAST signal from 27P which delays TBCO output from IC1 — 17P.

- **CD/CDV play**

The operation of CDV video play sections is exactly the same as for LD video play.

During the audio play sections of CD or CDV, CD SPDL error is input to the absolute value amp IC7 on the VSOP Assembly (TBC section) and the SPDL motor driven.

6.2. SUMMARY OF SPDL & TBC

	CLD-3070
SPDL error detection CCD/CPC error detection	} PD6064A + PA5012
SPDL REF-H	T.S.S. (regardless of memory ON/OFF)

Frequency phase errors and CCD errors are detected by using the trapezoid generated from REF-H (Reference-H-synch) and PB-H (Playback-H synch), as well as the method of reference shift which delays REF-H by either 28μsec or 36μsec when necessary. Furthermore, spindle and CCD servos are always operating at the same time.

During SCAN and other operations, when the TRKG servo loop is open, REF-H is being held. And when the servo loop is closed, REF-H is activated in phase with PB-H. The fact that SPDL servos and CCD servos are turned on at the same time after a jump, with the CCD servo operating until the SPDL motor has been able to absorb frequency component errors, allows the color lock to be activated immediately after a jump.

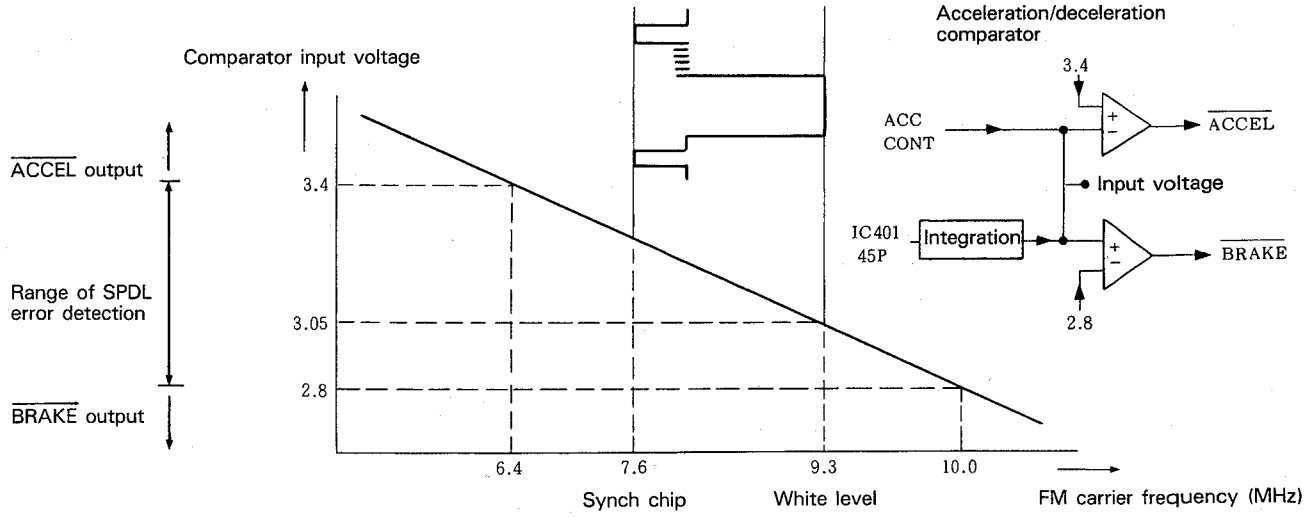
Consequently, in the CLD-3070, since the TSS signal, which is the 576fH, A/D, D/A conversion clock of the video memory section, undergoes frequency division by 576 at PDJ002, is being employed, memory ON/OFF no longer has any bearing on the status of REF-H..

6.3 DETECTION AND CONTROL OF RUNAWAY SPDL MOTOR

In cases where the SPDL motor runs out of control, if the number of revolution of the SPDL motor for whatever reason get out of the servo's tracking range, speed can be controlled by using either acceleration ($\overline{\text{ACCEL}}$) or deceleration ($\overline{\text{BRAKE}}$) signals.

In this manual, voltage inversely proportional to the video FM carrier frequency in the RF signal from the screen image demodulation section is extracted and input to the acceleration/deceleration signal detection comparator.

The output of IC202 (PA5010) — 45P of the VSOP Assembly (VDEM) is integrated and input to the comparator of IC201 (NJM2903S). The input voltage to the comparator is as shown in the figure below.

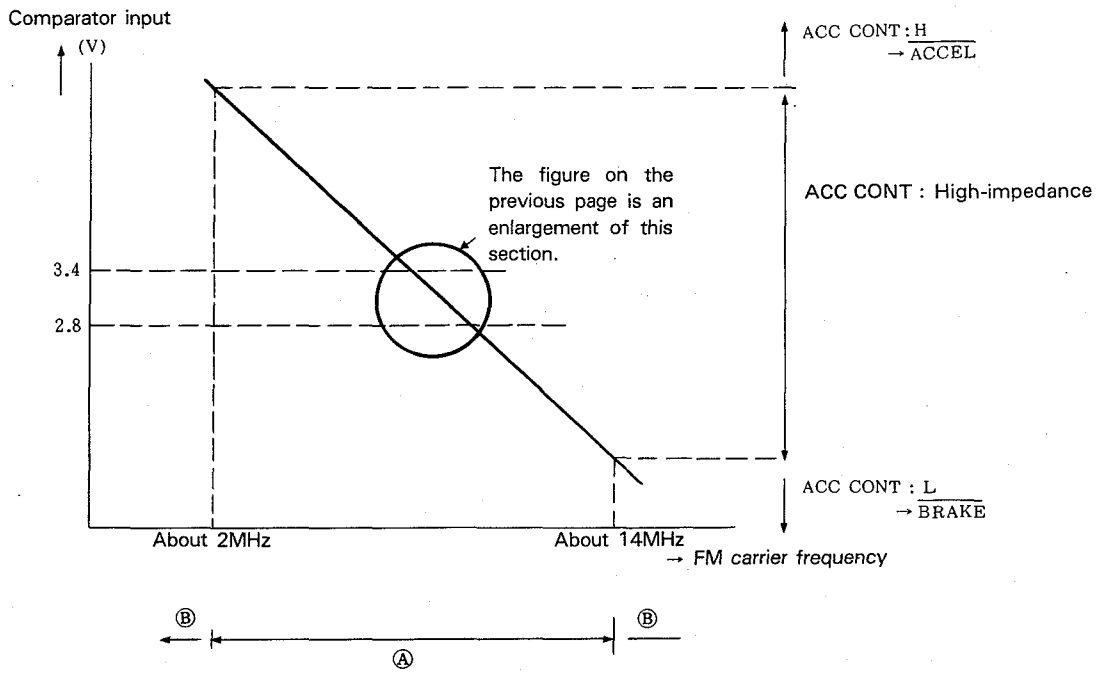


When the FM carrier frequency is at the 100% white level, equivalent to 9.3M, the comparator input voltage is at 3.05V. The upper and lower threshold voltage levels are then set at the detection limits of the SPDL servo frequency error. The $\overline{\text{ACCEL}}$ signal is over 3.4V and the $\overline{\text{BRAKE}}$ signal is under 2.8V. Both are labeled L.

Detection works on the basis of DC voltage when the SPDL servo LOCK goes out of order and rotational speed is thrown off. $\overline{\text{ACCEL}}$ or $\overline{\text{BRAKE}}$ signals are output when disc speed goes beyond the tracking range of the servo. These oblige the spindle motor to accelerate or decelerate until rotational speed again falls within the range of servo control.

When the outer tracks of a CLV disc are being played and the SPDL motor is rotating relatively slowly, it may be possible, if the SPDL servo is locked, to detect acceleration or deceleration signals being used to maintain the FM carrier frequency within the range shown in the figure above.

However, if the LOCK goes out of order and SPDL motor rotation is radically disrupted, the relation between frequency and DC voltage becomes non-linear and detection is no longer possible.



For this reason, the FG output cycle of the SPDL motor is measured by the system microprocessor CPU. If it falls into the areas marked B in the figure below, i.e., beyond 80% of reference speed, ACC CONT (ACCEL CONTROL) which is input to the acceleration/deceleration comparator registers either H or L and SPDL motor speed control is performed by the CPU.

In addition, the system microprocessor CPU also performs SPDL motor stop detection at the conclusion of play based on the FG output cycle.

When rotational speed is within 80% of reference speed (the area marked off as A in the figure below), the ACC CONT signal is in a Hi-Z state and speed control is not performed by the CPU.

7. FOCUS (FOCS), TRACKING (TRKG), SLIDER (SLDR) AND TILT SERVOS (DESCRIPTION OF THE HA11529).

7.1. SUMMARY

The HA11529 is an analog/digital hybrid bipolar IC which performs the following functions:

1. FOCS servo control (FOCS servo loop pull in control, FOCS servo loop gain control)
2. TRKG servo control (TRKG servo loop ON/OFF and brake control of spindle motor rotation during track jump and SCAN operations)
3. SLDR servo control (SLDR servo loop ON/OFF, variable speed transport, motor PWM drive)
4. TILT servo control (TILT servo loop ON/OFF)
5. CD/LD FOCS and TRKG servo switch
6. All of the above functions are controlled by 8-bit serial data passed through a serial bus (DATA, CLK, LATCH).
   The 8-bit serial data commands are as shown below.

MODE	ADDRESS				DATA			
	D7	D6	D5	D4	D3	D2	D1	D0
SCAN MODE CONT	1	0	0	0	SCAN SPEED 1	SCAN SPEED 2	SCAN SPEED 3	1: SCAN ON 2: SCAN OFF
SERVO CONTROL 1	1	0	0	1	FOCS 1: ON 0: OFF	DIRECTION 1: FWD 0: RVS	TILT 1: ON 0: OFF	1: LD 0: CD
SERVO MODE CONTROL 2	1	0	1	0	TRKG Zero cross output 1: 1/256 0: Through	TRKG 1: OFF 0: ON	TEST 1: TEST 0: NORMAL	—

* It is possible to set SCAN SPEED at 7 stages using the 3 bits, D3/D2/D1.

7.2. HA11529 Pin Functions

Pin No.	Pin Function
1.	Vee: −5V
2.	FOCS ERROR signal input: OP AMP input to which a SW is connected for gain control during SCAN operation
3.	FOCS SUM input: For DISC detection. Comparator input threshold is +0.4V.
4.	Comparator input threshold for the FOCS S-curve detection is +0.3V.
5.	Comparator input threshold for MAIN BEAM ON/OFF track detection is +0.5V. FOCS SUM input.
6.	TRKG ERROR input: Comparator input threshold for TRKG ERROR zero cross detection is 0V.
7.	GND
8.	TRKG ERROR AMP for CD input
9.	TRKG ERROR AMP for LD input
10.	TRKG ERROR AMP output. TRKG servo phase compensation is connected between this pin and pins 8, 10.
11.	Output for switching the TRKG servo loop characteristics during track jump. (Open or Close)
12.	Outputs the actuator drive and brake pulse during track jump and the actuator brake pulse during SCAN.
13.	Window comparator input to detect the amount of movement in the TRKG actuator during SCAN. Threshold voltage is 0.2V. Actually, an FTS SCAN signal is being input.
14.	Current setting terminal for TRKG actuator brake.
15.	Current setting terminal for pins other than 14P
16.	TRKG RTN input: TRKG RTN input for SLDR servo.
17.	SLDR servo amp output: During play, the SLDR motor is PWM driven and at that time this pin becomes the window comparator input.
18.	SLDR drive signal output during play or when high speed slider is in operation.
19.	SLDR drive signal input when SLDR is operating at low or mid speeds.
20.	Capacitor connected pin for setting the slope of the reference triangular wave for the SLDR motor PWM drive during play.
21.	Resistor-connected pin to set comparator threshold for turning off the TILT servo drive.
22.	TILT ERROR input: op amp input.
23.	A VR is connected for setting the TILT servo gain with the output of the op amp from 22P.
24.	Output for TILT motor drive.
25.	T-CROSS output: TRKG ERROR zero cross count output. Depending on the serial data command, output may be divided by 256.
26.	$\overline{\text{F-LOCK}}$: L when FOCS lock activated.
27.	J-TRIG input: triggered at startup. L under normal operating conditions.
28.	$\overline{\text{RESET}}$ input:
29.	$\overline{\text{LATCH}}$ input: serial interface bus to the system microprocessor CPU. (29, 30, 31P) Data is latched on the trailing edge.
30.	SDATA input: 8-bit serial command data input.
31.	$\overline{\text{SCLK}}$ input: clock for serial data transmission.
32.	500kHz input: internal logic clock input.
33.	TEST pin: normal state = L.
34.	Pin for setting the injection current used by internal I^2L logic.
35.	Capacitor connected pin for setting the lens UP/DOWN cycle when FOCS ON is activated.
36.	Drive voltage output for lens UP/DOWN.
37.	FOCS Error amp output: FOCS servo phase compensation is connected between 38, 39P.
38.	FOCS Error LD input.
39.	FOCS Error CD input.
40.	Pin with connected offset adjustment VR that uses the uninverted FOCS Error amp input
41.	Op amp output for FOCS gain control
42.	Vcc: +5V.

7.3. DESCRIPTION OF FUNCTIONS

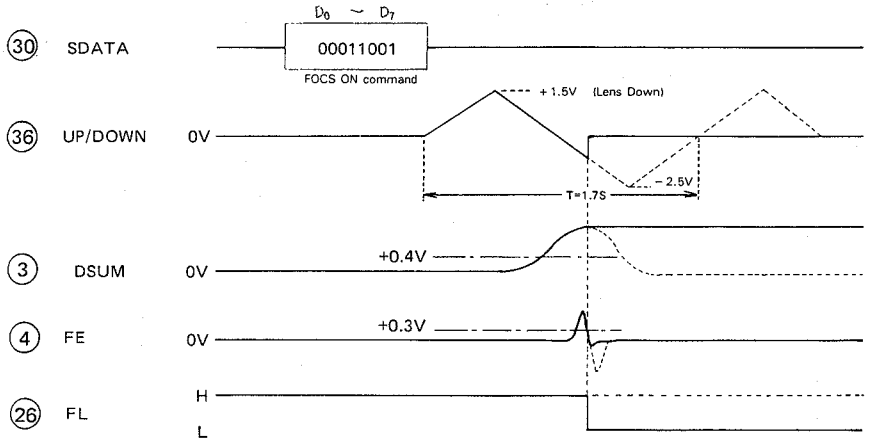
7.3.1. FOCS Assembly

1) FOCS pull in operation

The pull in operation of the FOCS servo raises the objective lens UP/DOWN and, when the input of DSUM (pin ③) and FE (pin ④) fulfill FOCS lock conditions, turns the FOCS servo loop ON. In the case of a defocus caused by damaged disc, the FOCS servo loop is turned OFF and, about 0.5 seconds later, a voltage of +0.6V is output at pin 36.

2) FOCS down and repeat pull in

When the input of DSUM (pin ③) falls below +0.4V as a result of a damaged disc or excessive external vibration, the unit detects an abnormal condition. When this occurs the FOCS servo loop is turned off and at the same time the objective lens is automatically moved UP/DOWN. When conditions as described in 1) have been fulfilled the FOCS servo loop turns to ON.



* The dotted line indicates the wave form when the FOCS servo loop is not ON.

Fig. 7-3-1 FOCS Servo pull in Timing Chart

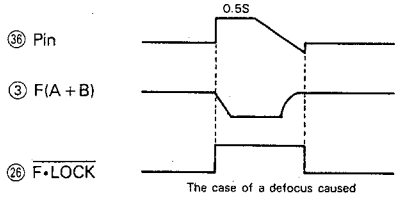


Fig. 7-3-2 Defocus Timing Chart

3) CD/LD switching

Depending on what type of disc is being played, compact disc or laser disc (CD or LD), a switch alters the loop gain and phase compensation of the FOCS servo for the particular disc type. The serial data bit for the CD/LD switch has the same address as the FOCS ON command bit and both can be set with a single transmission.

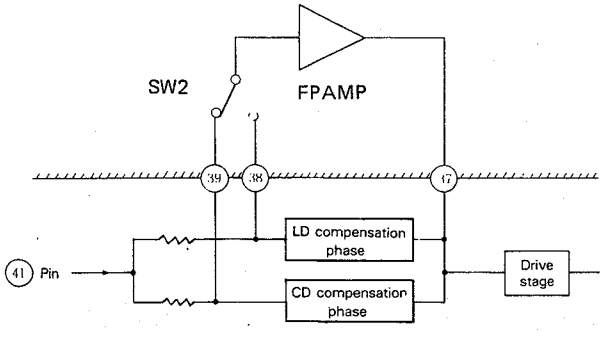
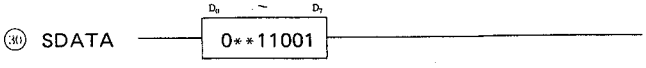
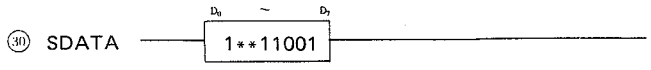


Fig. 7-3-3 CD/LD switching

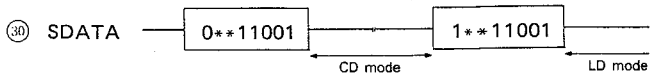
i) Focus ON command when the CD mode is set.



ii) FOCS ON command when the LD mode is set.



iii) When the CD/LD mode is switched in the middle of playback (CD mode → LD mode)



Note 1) The asterisks (*) represent bits which bear no relation to the operation under examination. (This convention will be used throughout the manual.)

7.3.2. TRKG Assembly

1) Track jump operation

Track jump commences when the jump trigger startup pulse is received from JUMP (pin ㉗). Acceleration and deceleration switching are performed by monitoring tracking error zero cross. During a jump operation, SW12 and SW24 are activated sequentially. SW12 is used to switch TRKG loop characteristics and SW24 for adjusting the position of TRKG error zero cross.

Switching between forward and reverse jump is performed by serial data transmission.

The jump trigger signal, controls so that the phase of the input signal to 6P can be pushed forward beyond its position during normal operation.

i) Forward jump

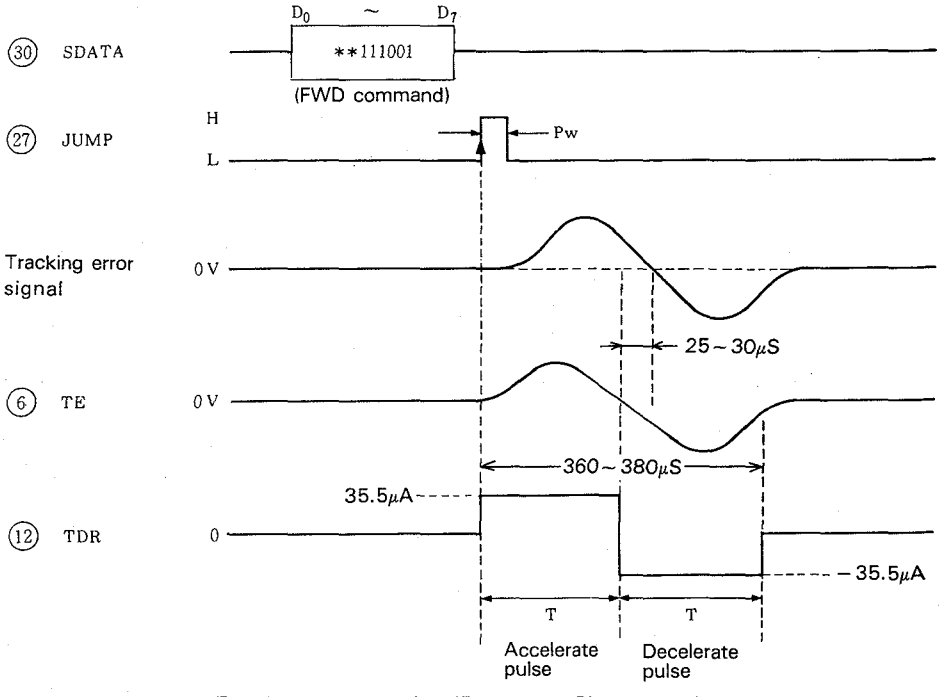
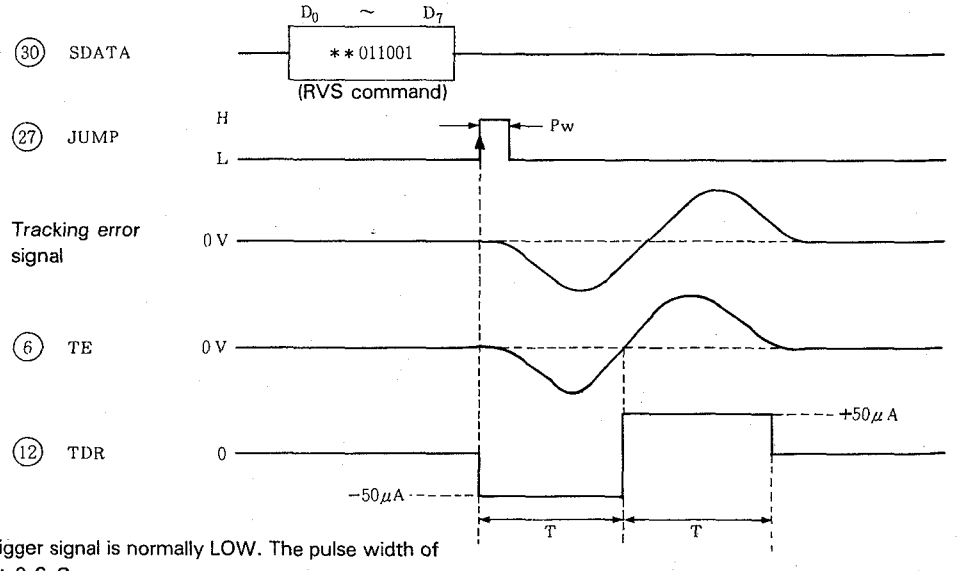


Fig. 7-3-4 FWD JUMP Timing Chart

ii) Reverse jump



Note 1) The jump trigger signal is normally LOW. The pulse width of Pw is set at 9.6μS.

Fig. 7-3-5 Reverse jump Timing Chart

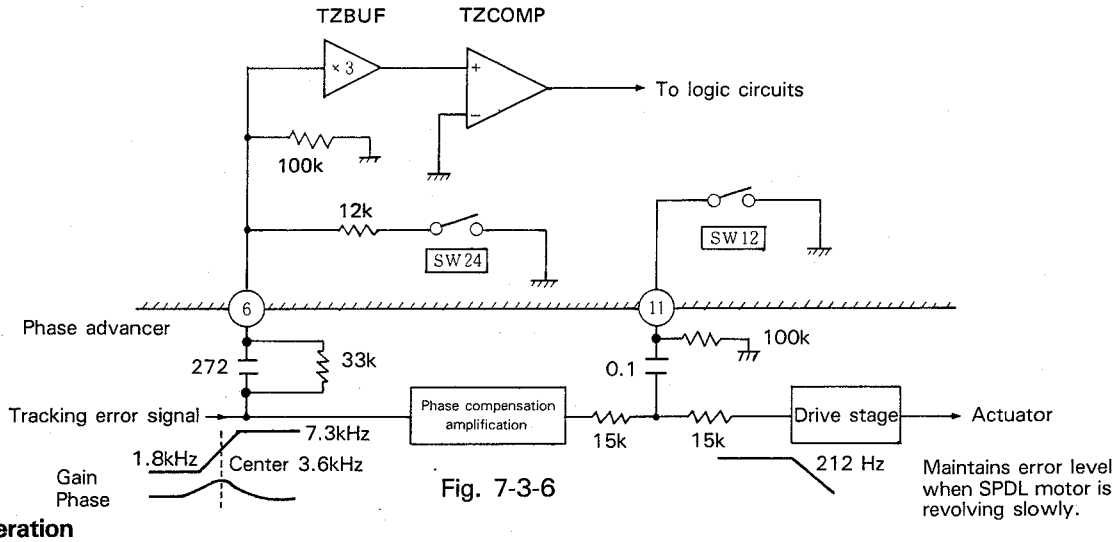


Fig. 7-3-6

2) Scan operation

During slow or medium scan the TRKG servo performs ON/OFF control of the TRKG loop. Input to ST (pin ⑬) signals displacement of the actuator position and the TRKG servo loop is turned OFF. When the error signal at TE (pin ⑥) drops below a set frequency, the TRKG servo loop is turned back ON.

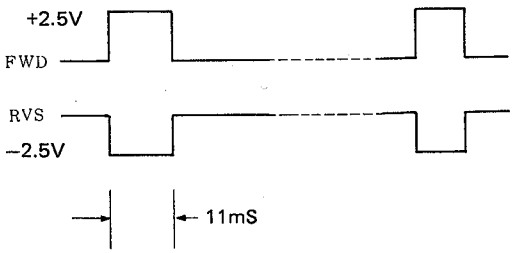
While the TRKG servo loop is OFF, a brake pulse is output by TDR (pin ⑫) according to the timing charts shown below. The polarity of the brake pulse is not a direction command sent via serial data but is determined by the polarity of the signal input to ST (pin ⑬). Corresponding to actuator speed as detected by TE (pin ⑥), brake pulse duty is automatically set to operate in 5 stages (50%-100%). Brake current IB can be adjusted at BSET (pin ⑭).

Because switch timing for the open/close operation of the TRKG servo loop during SCAN is determined by the system microprocessor, an FTS signal like that shown below is actually input to pin ⑬.

This signal also flows into pin ⑫, but the polarity of the brake pulse is opposite to it, which acts to improve convergence during braking.

The cycle of the FTS SCAN signal varies depending on the absence or presence of video memory.

After a jump, the TRKG servo loop closes and if one field worth of data has been properly written to memory, the following FTS scan signal is output. To account for possible mistakes in writing to memory, the period for this operation is not fixed.



i) Forward scan

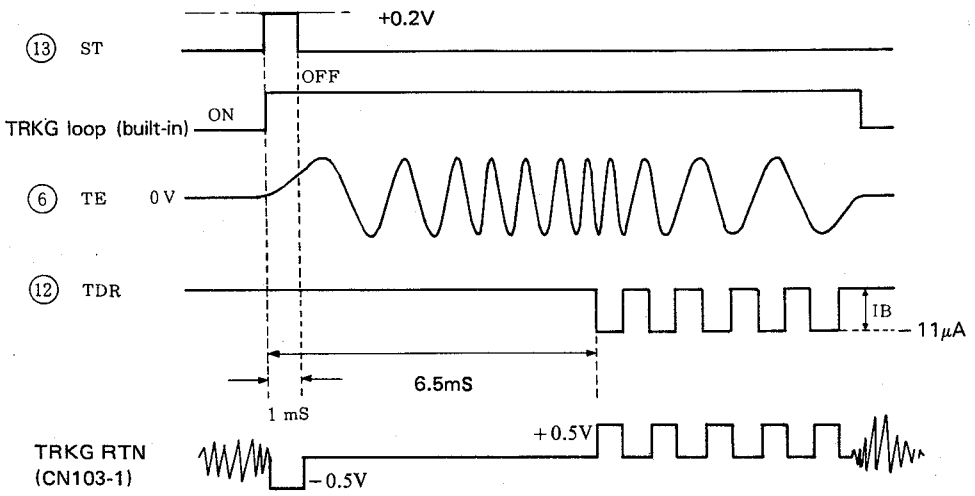


Fig. 7-3-7 Timing Chart of Forward scan

ii) Reverse scan

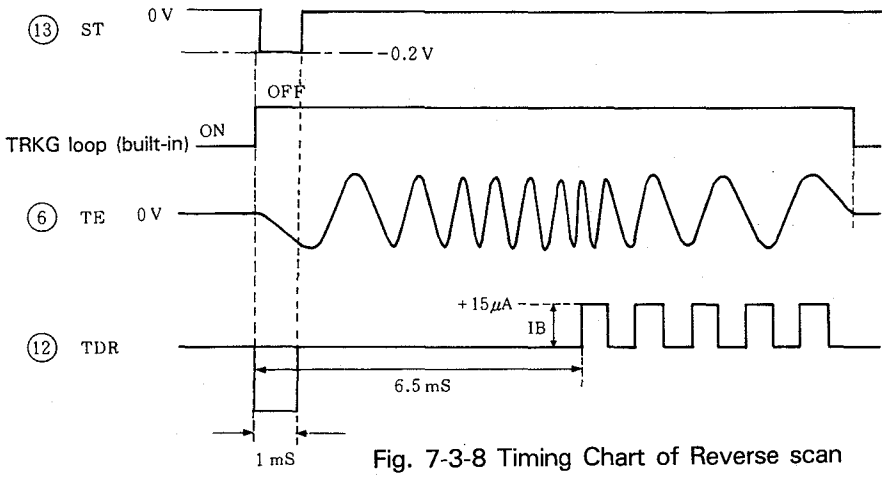


Fig. 7-3-8 Timing Chart of Reverse scan

3) CD/LD switching

Switching between CD and LD is performed in exactly the same way as CD/LD switching for the FOCS servo.

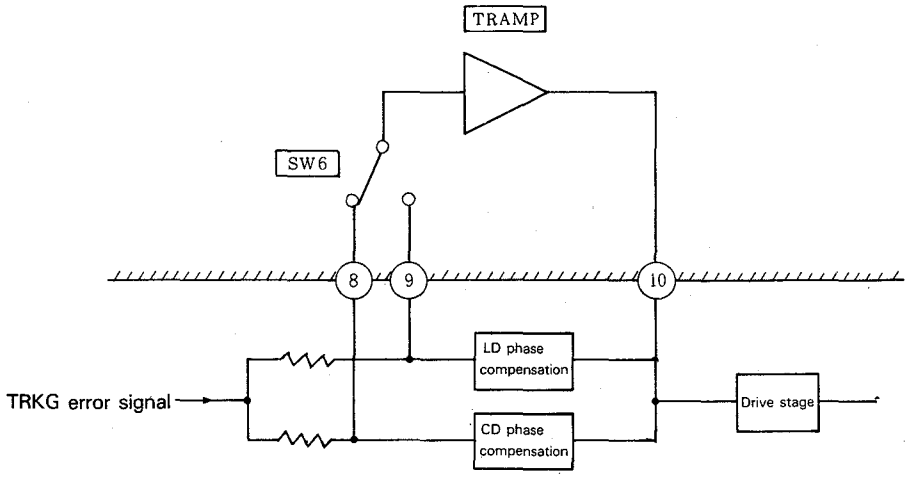


Fig. 7-3-9 CD/LD switching

4) TRKG servo loop ON/OFF control

Switching the TRKG servo loop ON/OFF is done by means of serial data transmission.

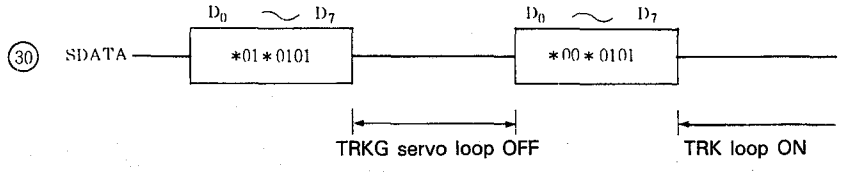


Fig. 7-3-10 TRKG servo loop ON/OFF

5) TRKG count

The number of tracks crossed during high speed scan is counted and then, according to the serial data transmission, a choice is made to either divide (1/256) the output TCNT (pin ㉕) pulse or output it as is.

When a misclamp is detected at the beginning of play, the pulse is divided (1/256) and when tracks are counted during CD search the pulse is output as is.

Once play has begun and the TRKG servo loop is open, track crossing is normal if the number of tracks crossed per disc rotation (6 FG pulses = 1 rotation) is under 1,280 tracks (TRKG count, 5 times: 1mm of eccentricity). If this number is exceeded, however, a misclamp is detected and the disc is ejected from the unit.

7.3.3. Slider Servo Operation

1) Operation in the normal play mode

During normal play DC components in the drive current of the TRKG actuator are PWM modulated at SCOMP1 and SCOMP2. This PWM pulse turns SW16 and SW17 ON and activates the output of the drive signal. The slope of the reference triangular wave can be altered by means of the capacitor connected to SLP (pin ⑳).

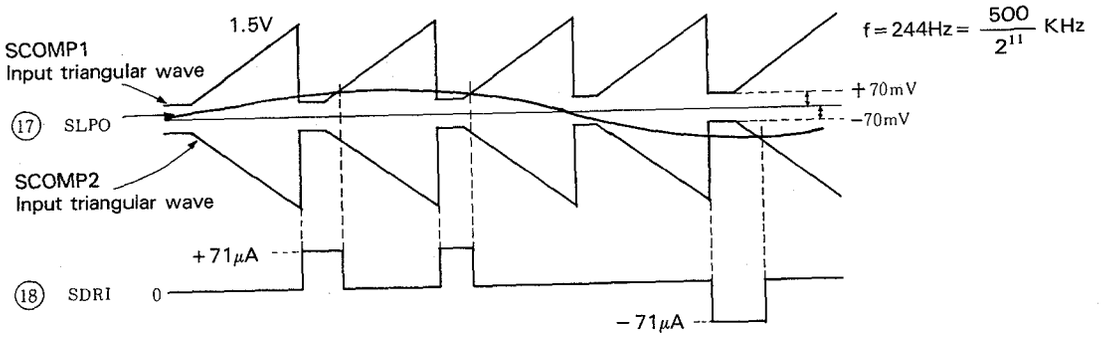


Fig. 7-3-11 SLDR Servo Operation

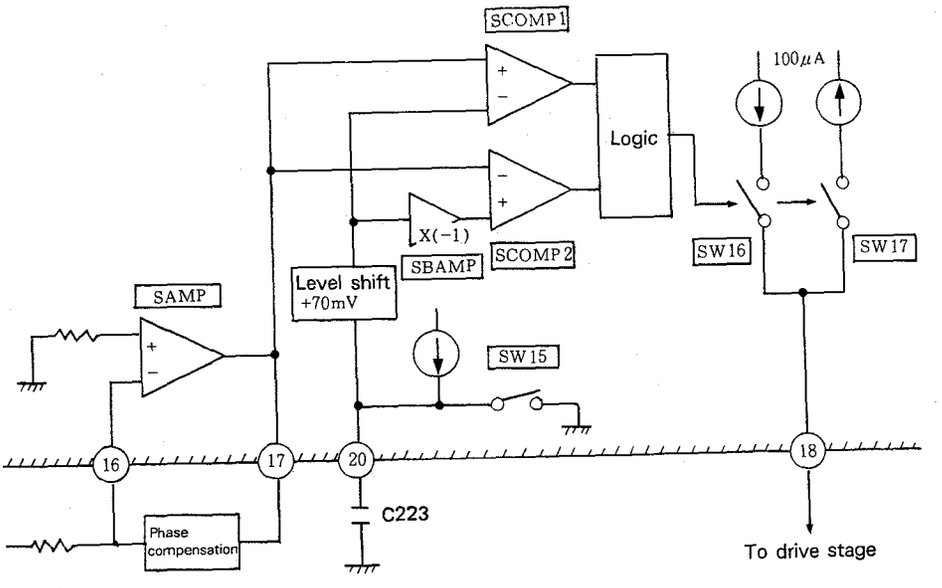


Fig. 7-3-12 SLDR Servo Part (HA11529)

2) Operation in the scan mode

During a scan operation, the SLDR servo loop is OFF and a signal that agrees with the set speed as given by serial data transmission is output either from SDR2 (pin ⑲) or SDR1 (pin ⑱).

i) Low and mid speed scan

SW18, SW20 and SW22 (when set in the FWD direction) or SW19, SW21 and SW23 (when set in the RVS direction) correspond to the serial data, D3, D2 and D1. When the bit is "0", it is OFF, and when the bit is "1", it is ON. Furthermore, on the basis of these three bit combinations a current of 10μA — 110μA (FWD) or −10μA — −110μA (RVS) is output as a duty 50% pulse from SDR2 (pin ⑲). Actually, however, when the unit is used as a CD player, only ±110μA is used.

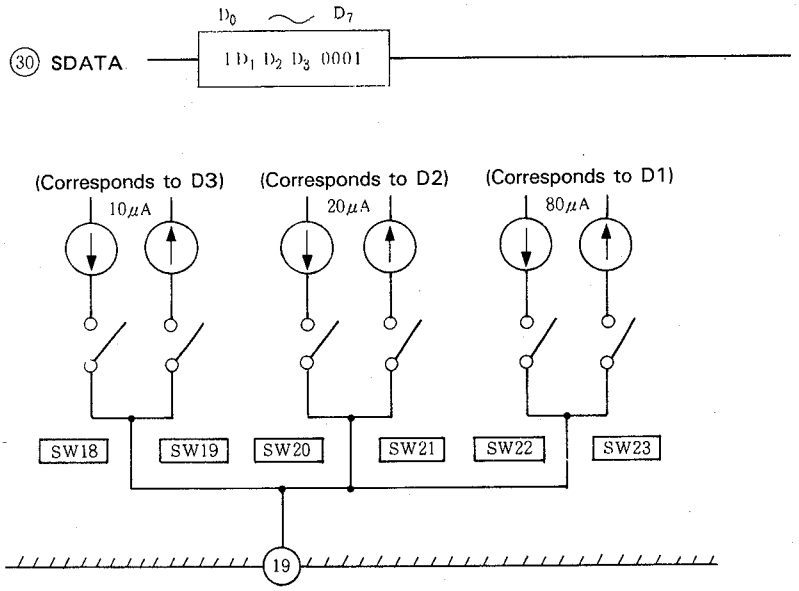
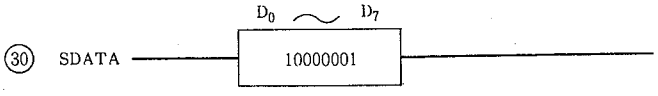


Fig. 7-3-13

ii) High speed scan

By means of the serial data transmission shown at the right, SW16 or SW17 can be turned ON and a ±100μA drive signal output from SDR1 (pin ⑱). The direction is as given in the serial data transmission.

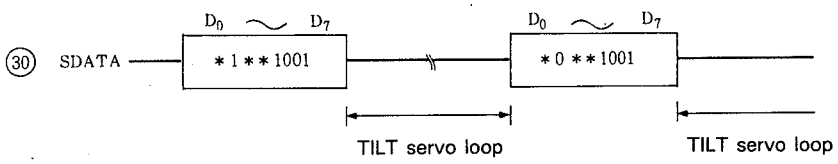


When the unit is used as an LD, the SCAN SPEED control function discussed above is not employed. A combination of the two commands, 10000001 for high speed SCAN and 10001110 that turns the SLDR servo loop OFF are used to control SLDR drive voltage and set SCAN SPEED.

7.3.4. TILT Assembly

1) Loop ON/OFF switch

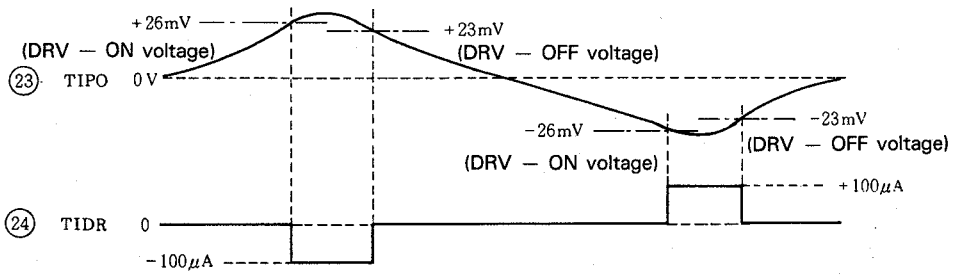
The ON/OFF control of the TILT servo loop is performed by means of serial data transmission.

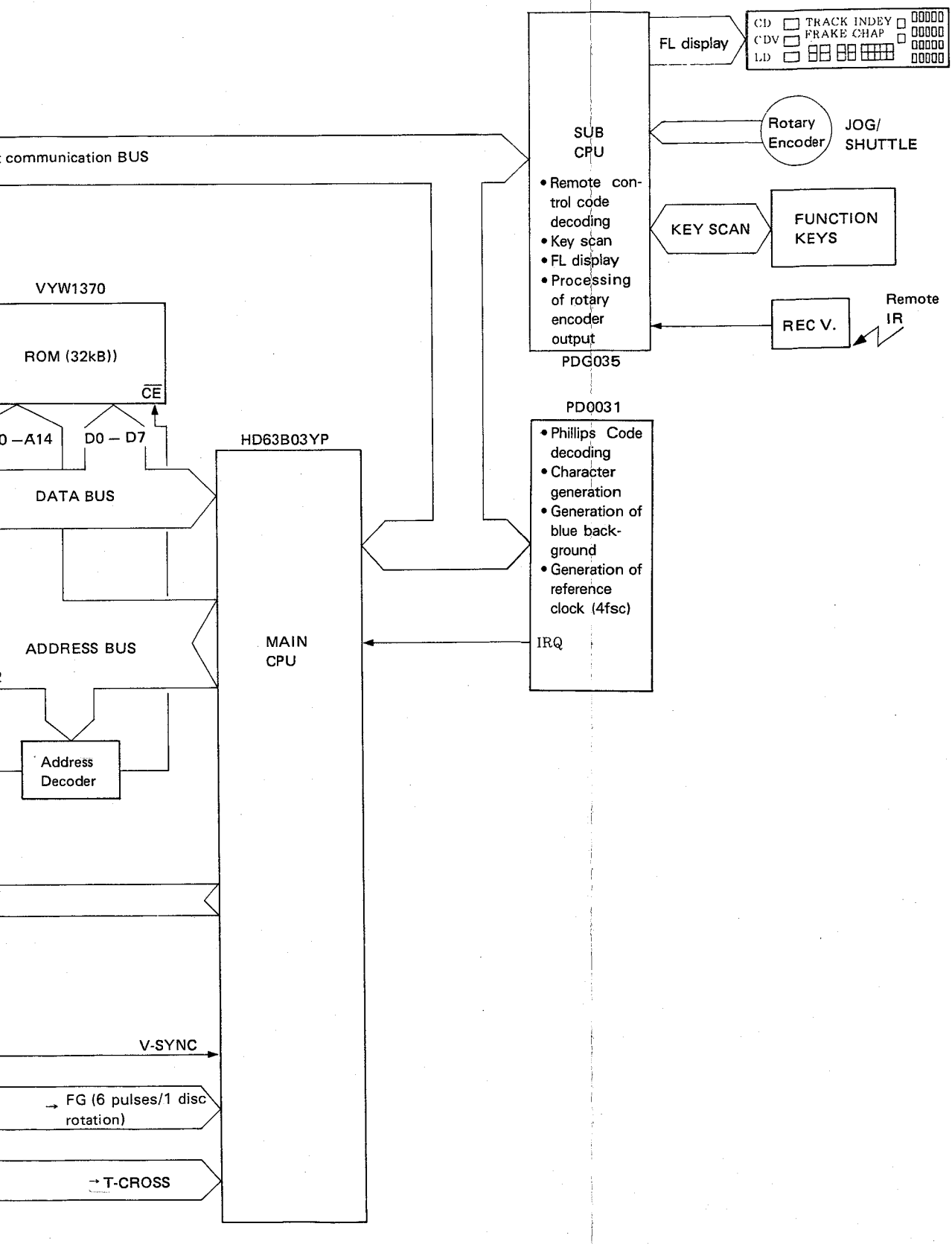


2) TILT servo operation

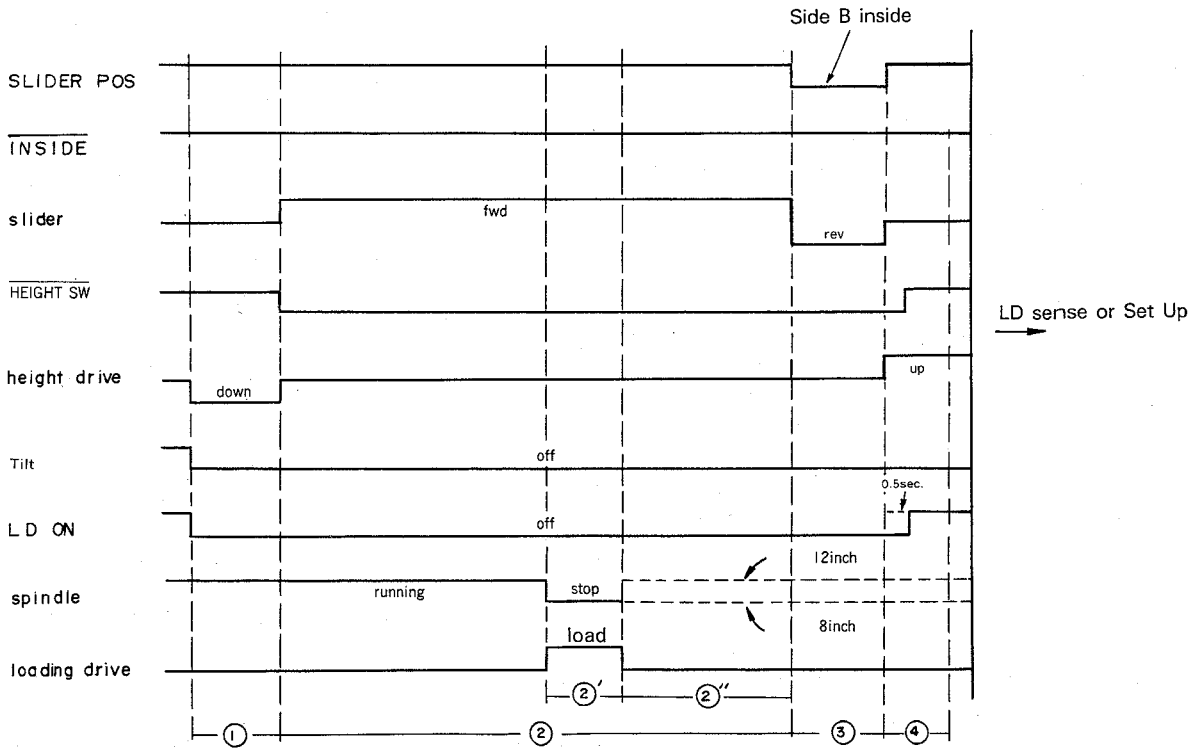
The TILT error signal is input to the window comparators TCOMP1 and TCOMP2. The drive voltage which is output at TSEF (pin ㉑) operates on an ON/OFF basis. If input is higher than the TCOMP2 reference voltage (DRV — ON voltage), then ON; if input is lower than the TCOMP1 reference voltage (DRV — OFF voltage), then OFF.

DRV — OFF voltage can be adjusted at TSEF (pin ㉑).




FL display
CD
CDV
LD
TRACK INDEX
FRAME CHAP
SUB CPU
• Remote control code decoding
• Key scan
• FL display
• Processing of rotary encoder output
PDG035
Rotary Encoder
JOG/ SHUTTLE
KEY SCAN
FUNCTION KEYS
REC V.
Remote IR
communication BUS
VYW1370
ROM (32kB))
CE
PD0031
• Phillips Code decoding
• Character generation
• Generation of blue back-ground
• Generation of reference clock (4fsc)
IRQ
0 –A14
D0 – D7
HD63B03YP
DATA BUS
ADDRESS BUS
MAIN CPU
Address Decoder
V-SYNC
FG (6 pulses/1 disc rotation)
T-CROSS

ching from side A play status to side B play
is:
eight motor is rotated in the direction in which
ickup is lowered.
e the slider is moved to the side B inside position,
tatus is monitored to see whether the spindle
r has stopped rotating or not.
n the spindle motor stops rotating, side B of the
is clamped.
en a 12-inch disc is loaded, the spindle motor
ts rotating.
the side B inside SW is turned ON, the slider
ved to the position where the side B inside SW
ned OFF.
e side B inside position, the height motor is
d in the direction in which the pickup is moved
d the disc. Then, after 0.5 sec. has elapsed after
on has started, LD ON signal is turned to H.



(3) Switching from side B play status to side A play status:

①The height motor is rotated in the direction in which the pickup is lowered.

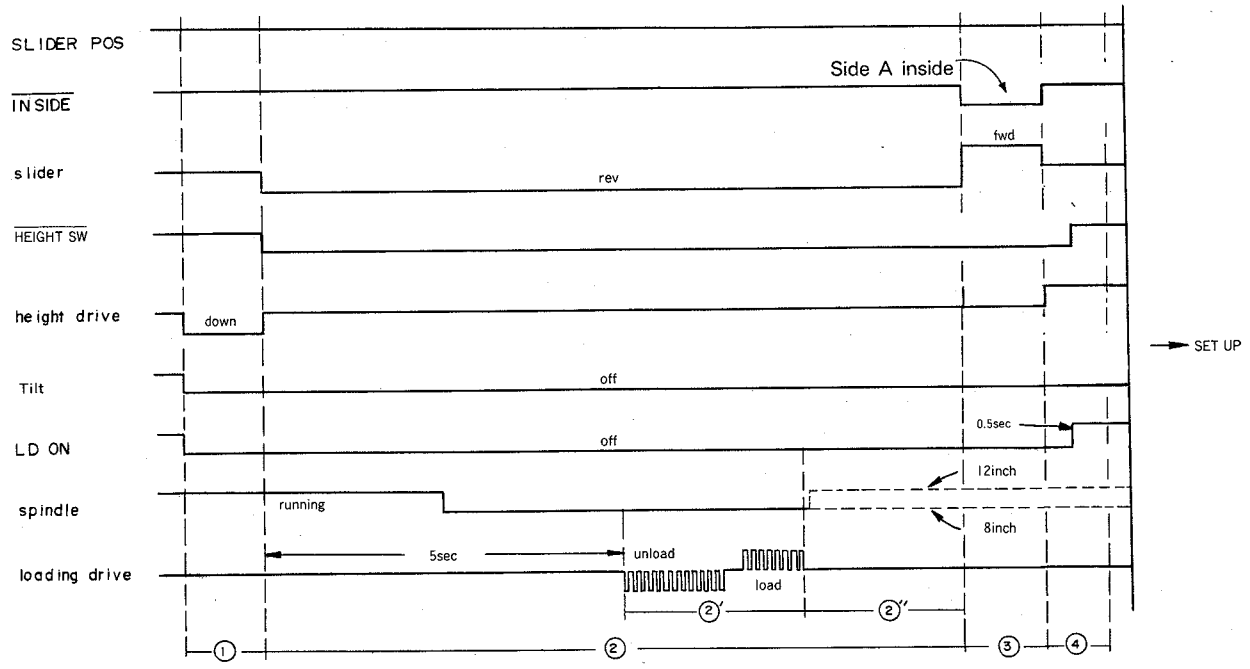
②While the slider is moved to the side A inside position, the status is monitored to see whether the spindle motor has stopped rotating or not. (Monitoring continues for 5 seconds even when rotation has stopped.)

②When the spindle motor has stopped rotating and 5 sec. has elapsed after the slider begins moving in the reverse direction, side A of the disc is clamped.

②" When a 12-inch disc is loaded, the spindle motor starts rotating.

③When the side A inside SW is turned ON, the slider is moved to the position where the side A inside SW is turned OFF.

④At the side A inside position, the height motor is rotated in the direction in which the pickup is raised. Then, after 0.5 sec. has elapsed after rotation has started, LD is turned ON.



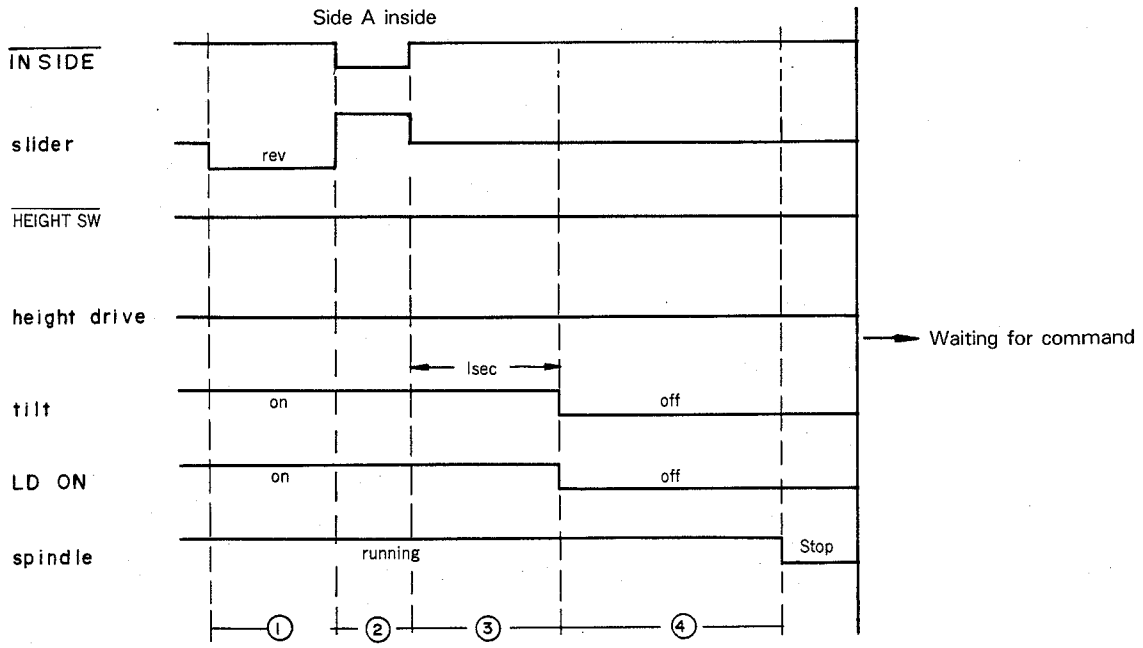
(4) Operation from the side A play status to the stop mode:

①While the LD tilt servo is operating, the slider is moved to the side A inside position.

②When the side A inside SW is turned ON, the slider is moved to the position where the side A inside SW is turned OFF.

③1 sec. later, the operation of the LD tilt servo stops.

④No operation will be performed until the spindle motor stops rotating.



(5) Operation from the side B play status to the stop mode:

①The height motor is rotated in the direction in which the pickup is lowered.

②When the slider has moved to the side A inside position, the status is monitored to see whether the spindle motor has stopped rotating or not.

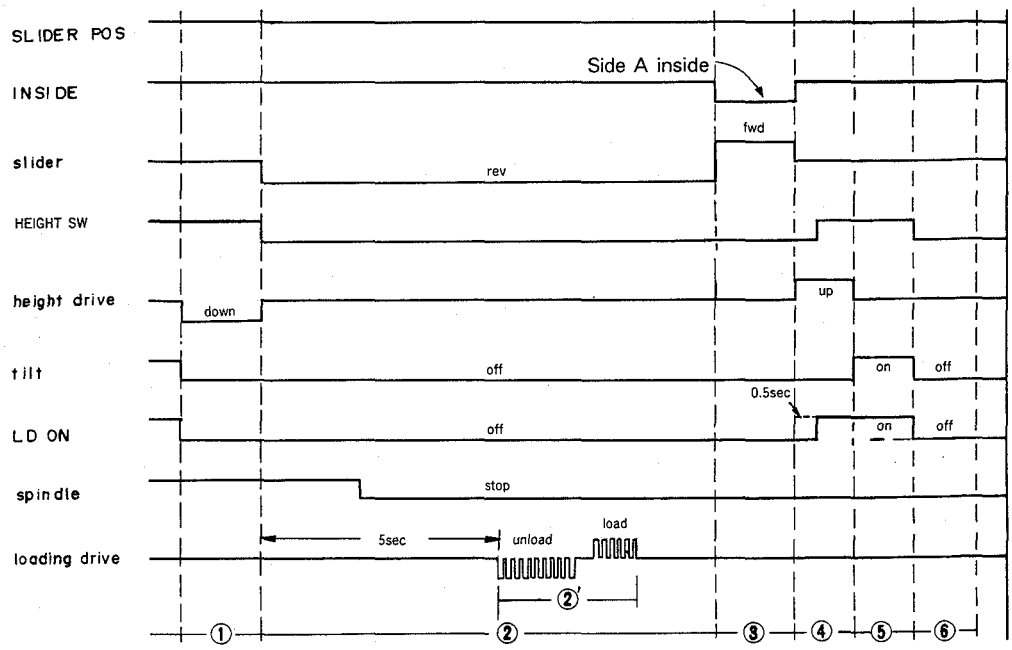
②'When the spindle motor stops rotating and 5 sec. has elapsed after the slider begins moving toward the reverse direction, side A of the disc is clamped.

③When the side A inside SW is turned ON, the slider is moved to the position where the side A inside SW is turned OFF.

④At the side A inside position, the height motor is rotated in the direction in which the pickup is raised.

⑤The LD tilt servo is turned ON and tilt adjustment is performed for side A (for 3 sec.).

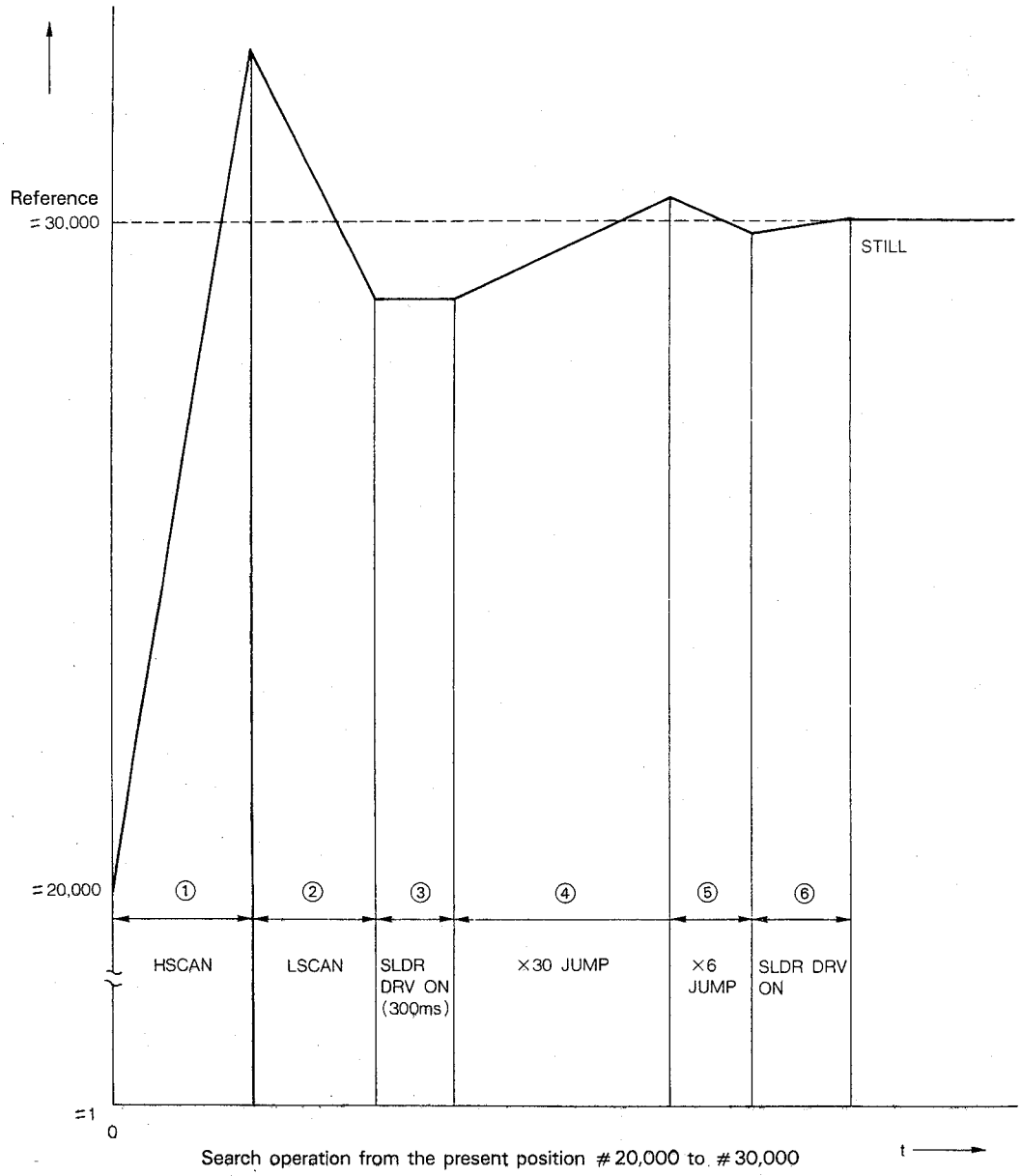
⑥The LD and the tilt servo are turned ON.



(6) When the power is turned ON:

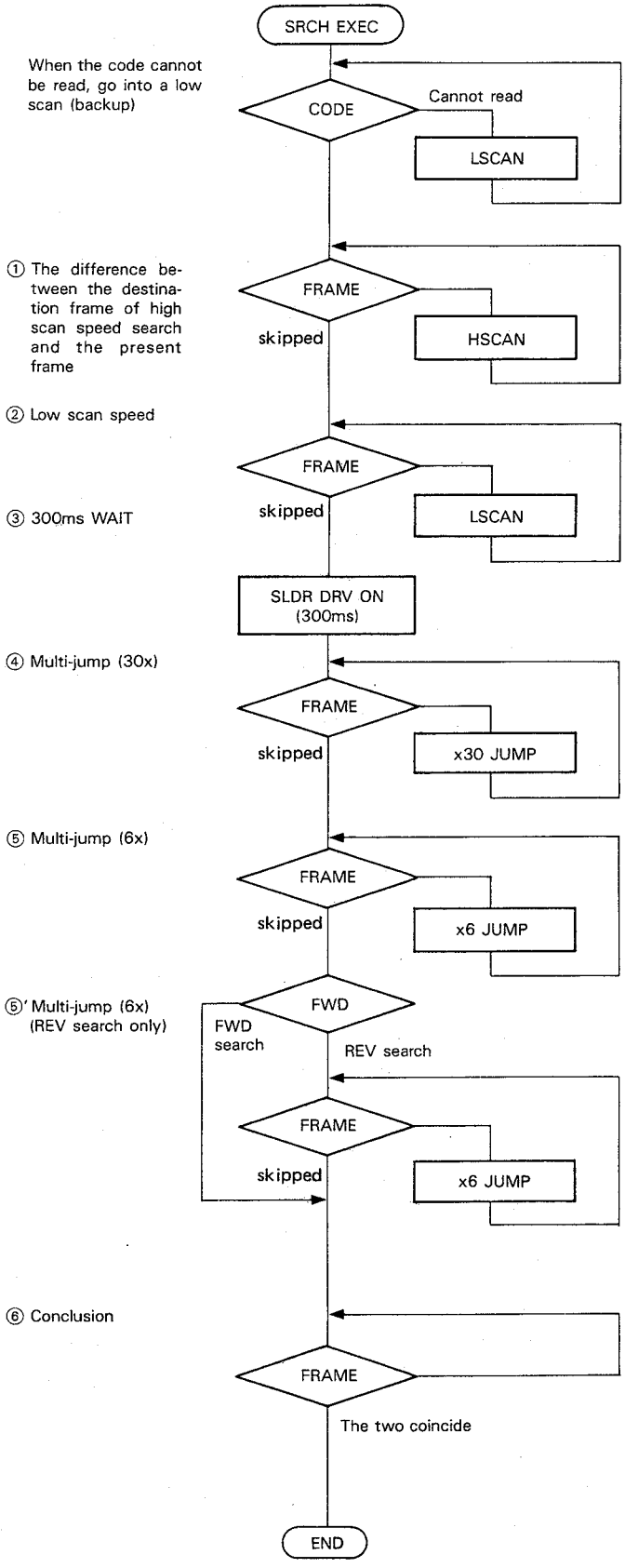
1) The height motor is rotated in the direction in which the pickup is lowered.
2) The height motor is rotated in the direction in which the pickup is raised for 1.4 sec.
3) As the presence of a disc or the type of disc, etc. before the power is turned OFF are stored in memory, after this, operation is performed according to the mode. That is, if an LD is loaded, the slider is stopped at the position where the LD inside SW is turned ON/OFF. If a CD is loaded, the TOC (table of contents) is read. If there is no disc, the slider is moved to the transportation position.

(7) Flame search operation

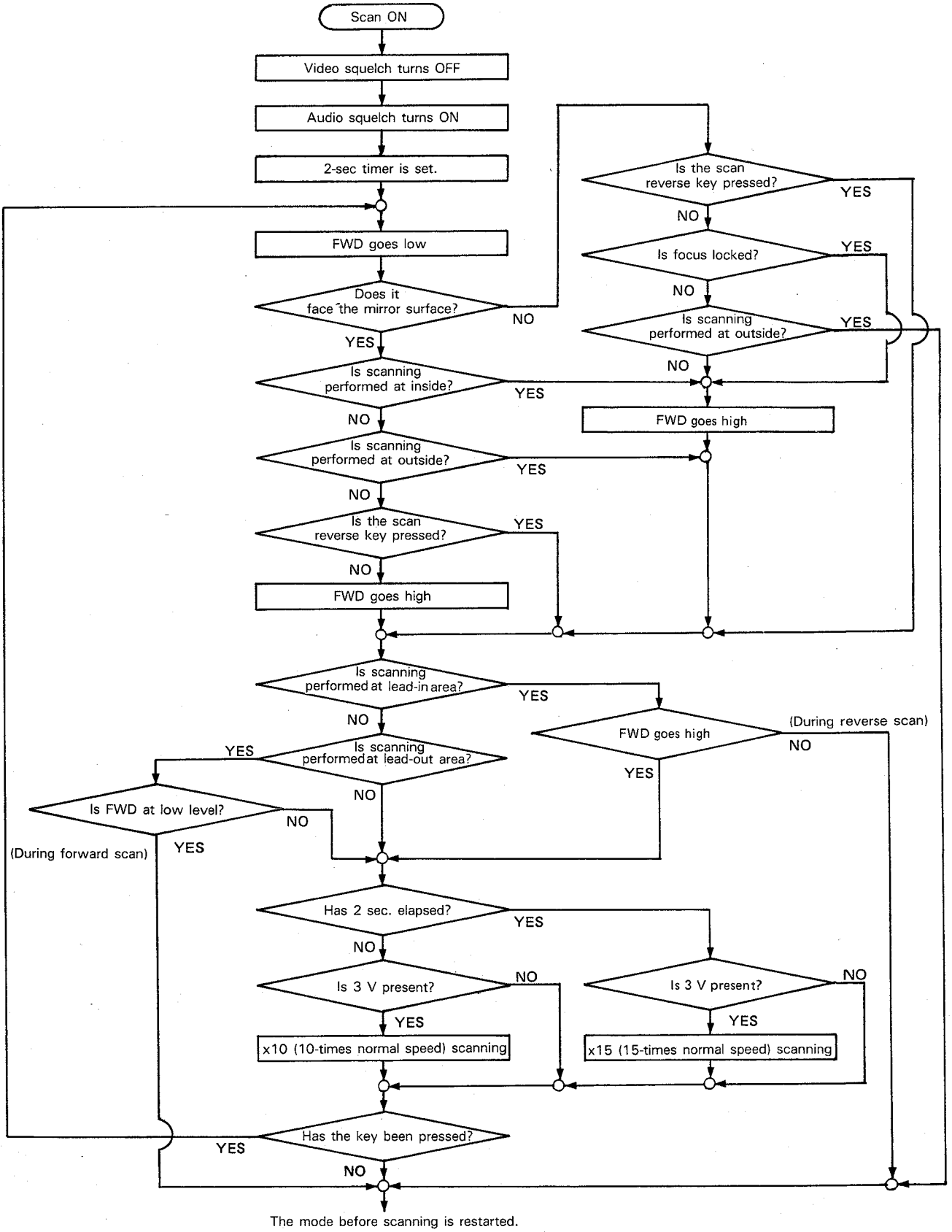


Flame search operation

Flow chart of frame search

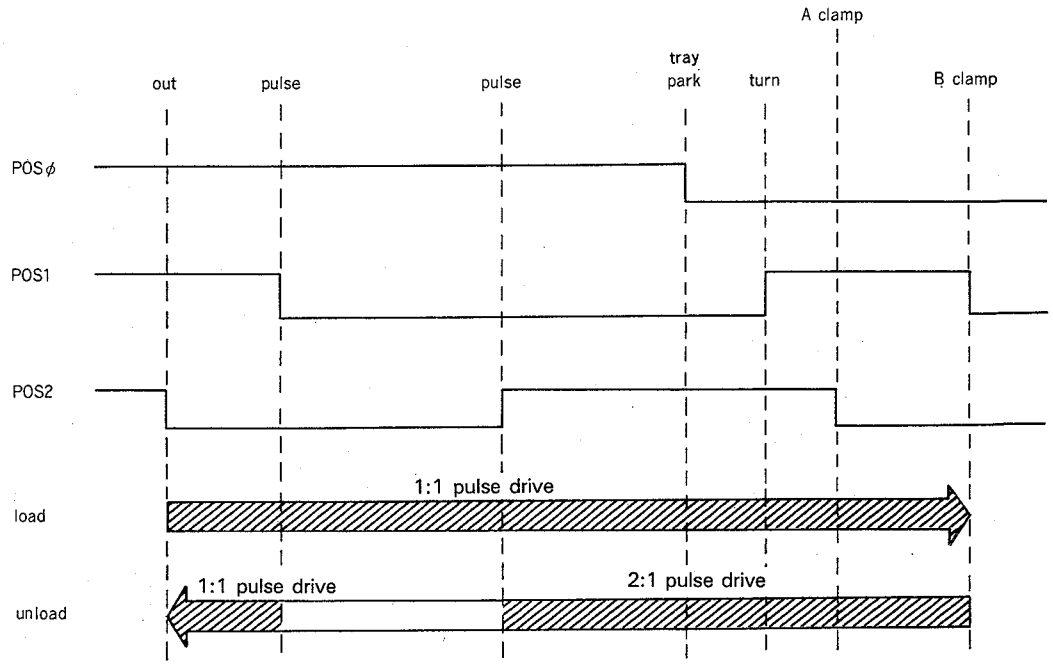


(8) Flow chart of scanning operation



(9) Loading operation:

To recognize the loading position, a rotary encoder is provided which outputs a signal using 3 bits to designate eight positions. The loading operation is performed by pulse drive according to the position detected by the above method.

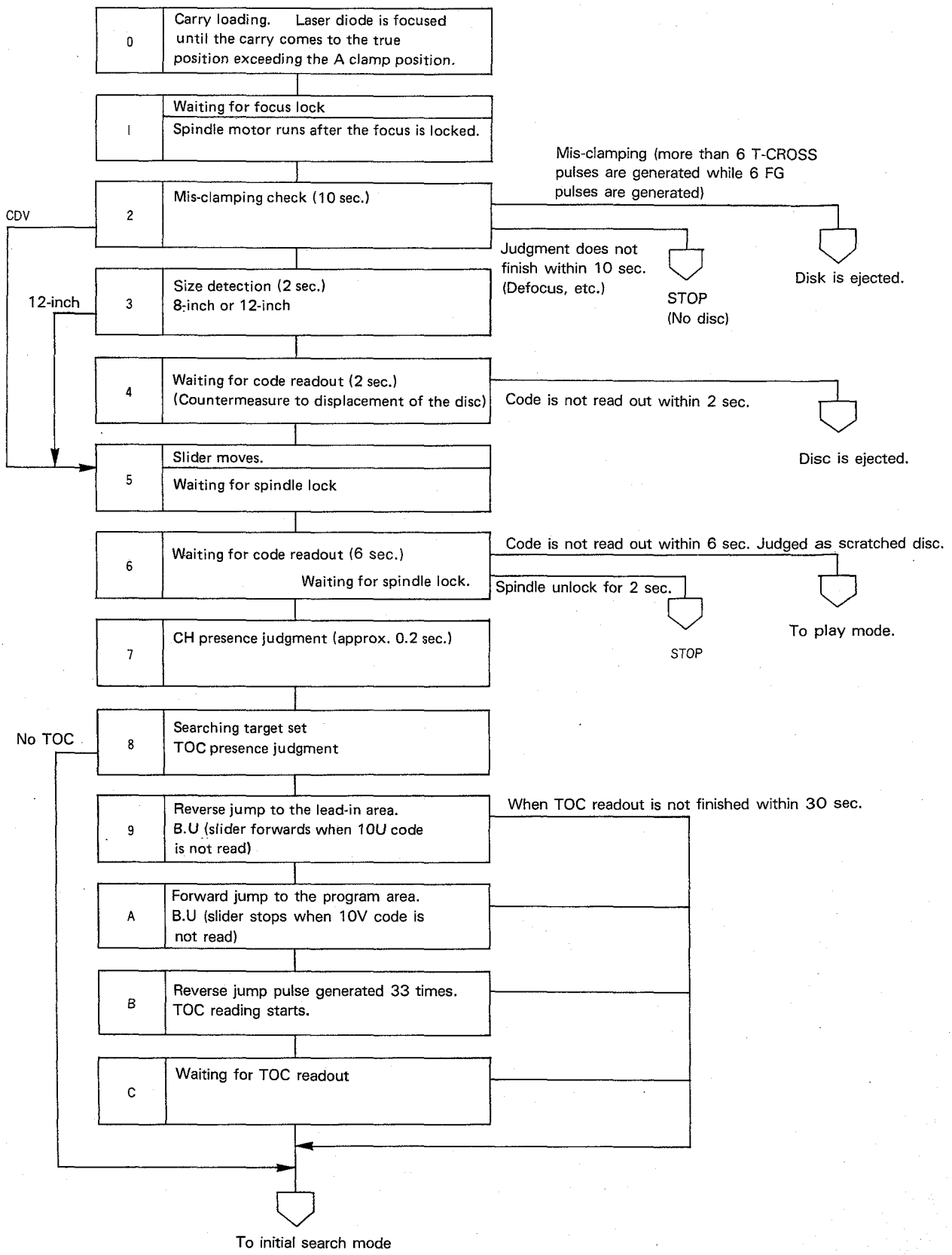


(10) Height servo:

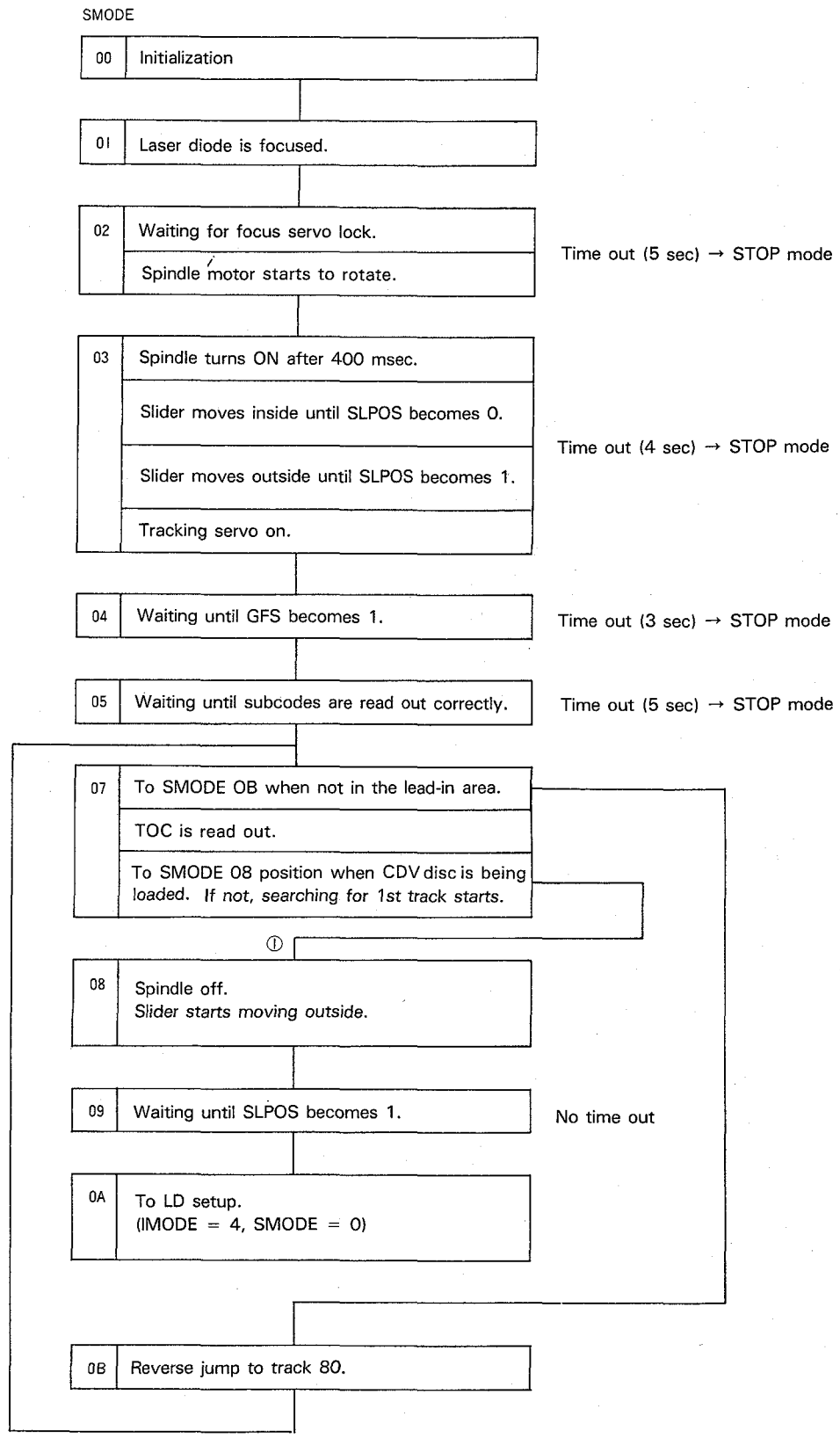
The height servo is used to obtain the sufficient focus stroke for any position on the disc. When LD (focus) is turned ON, it is controlled by the DC component of the focus servo signal. When LD is turned OFF, the height motor can be moved up/down under the control of the microcomputer.

The height servo is normally maintained in the condition of the disc which was played last. However, when the power is turned ON or when playback of the side B of the disc is finished, the height motor is lowered until the $\overline{\text{HIGHT SW}}$ signal is turned ON under the control of the microcomputer, then the height motor is raised (height neutral) after approx. 1.4 sec. has elapsed.

(11) LD setup (contents of SMODE display when IMODE = 4):



(12) CD setup:


SMODE
00
Initialization
01
Laser diode is focused.
02
Waiting for focus servo lock.
Spindle motor starts to rotate.
Time out (5 sec) → STOP mode
03
Spindle turns ON after 400 msec.
Slider moves inside until SLPOS becomes 0.
Slider moves outside until SLPOS becomes 1.
Tracking servo on.
Time out (4 sec) → STOP mode
04
Waiting until GFS becomes 1.
Time out (3 sec) → STOP mode
05
Waiting until subcodes are read out correctly.
Time out (5 sec) → STOP mode
07
To SMODE 0B when not in the lead-in area.
TOC is read out.
To SMODE 08 position when CDV disc is being loaded. If not, searching for 1st track starts.
①
08
Spindle off.
Slider starts moving outside.
09
Waiting until SLPOS becomes 1.
No time out
0A
To LD setup.
(IMODE = 4, SMODE = 0)
0B
Reverse jump to track 80.