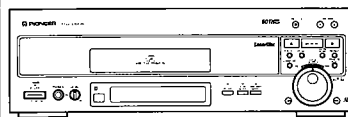


1793

PIONEER®
The Art of Entertainment

Service Manual



SERVICE GUIDE

ORDER NO.
RRV1066

CD CDV LD PLAYER

CLD-D703

CLD-D503

CLD-D770

CLD-D570

CLD-S360

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1. OVERALL BLOCK DIAGRAM

1.1 OVERALL BLOCK DIAGRAM FOR CLD-D503, CLD-D570 AND CLD-S360

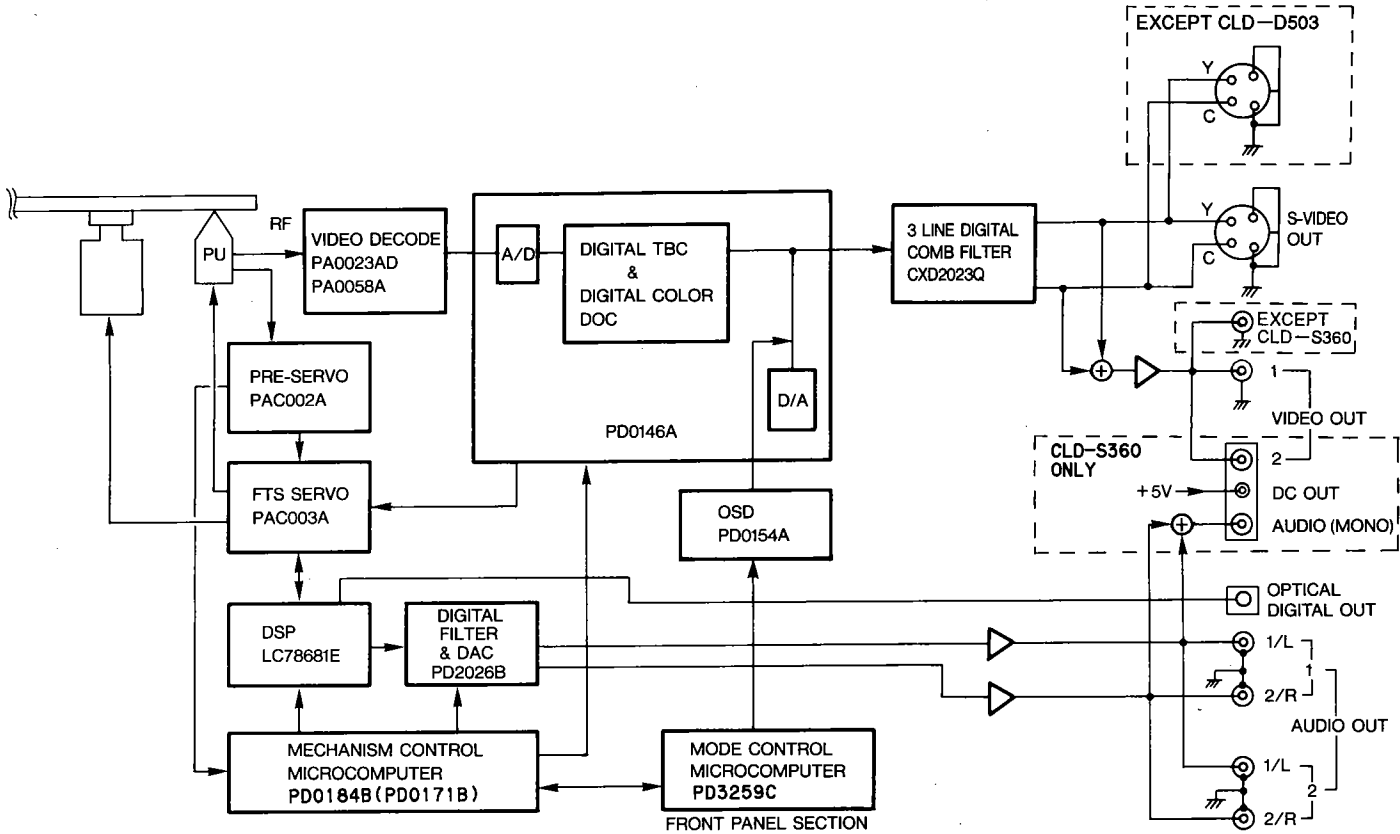


Fig. 1-1 OVERALL BLOCK DIAGRAM FOR CLD-D503, CLD-D570 AND CLD-S360

1.2 OVERALL BLOCK DIAGRAM FOR CLD-D703 AND CLD-D770

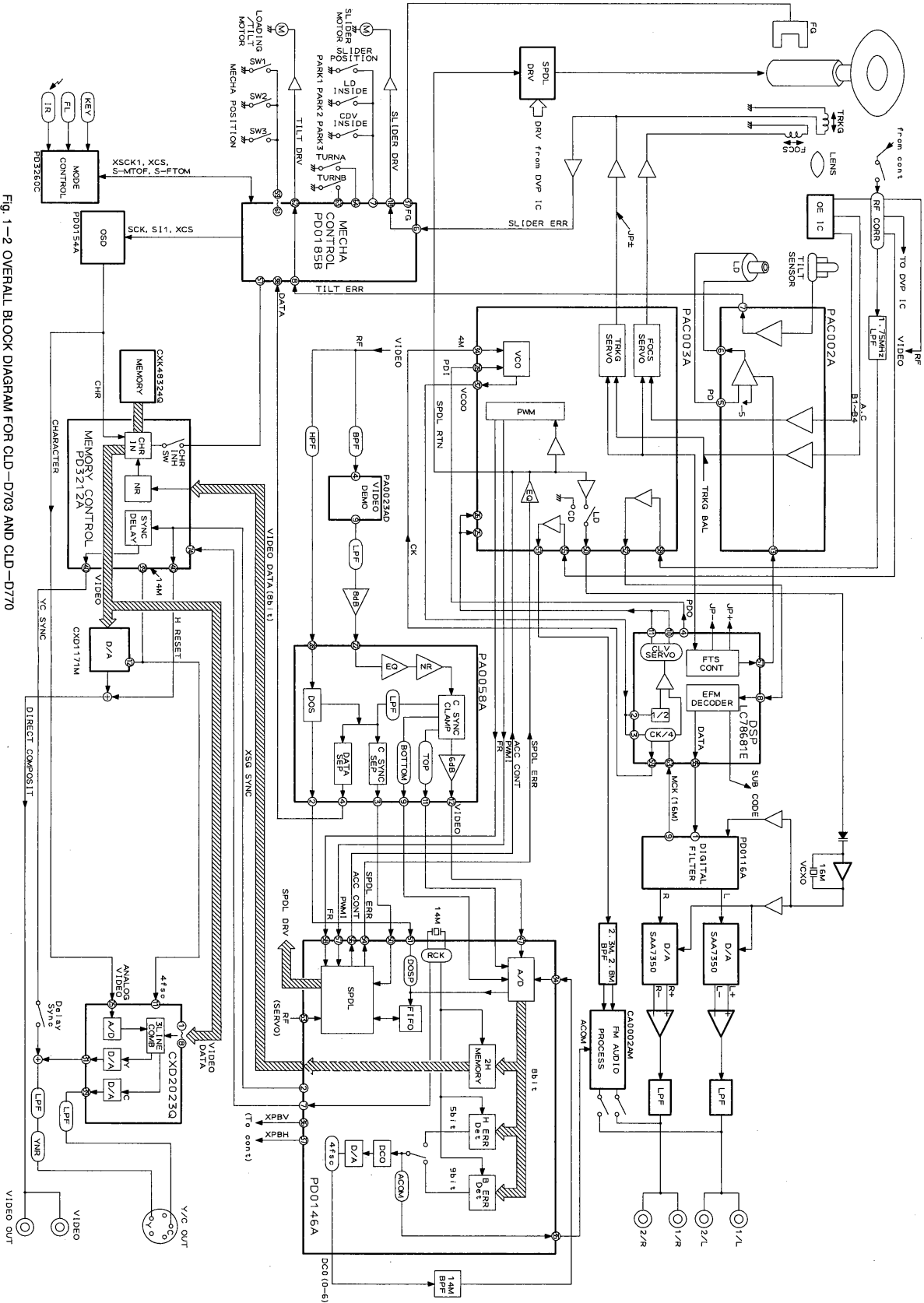


Fig. 1-2 OVERALL BLOCK DIAGRAM FOR CLD-D703 AND CLD-D770

CLD-D703, CLD-D503, CLD-D770, CLD-D570, CLD-S360

2. SYSTEM CONTROL DESCRIPTION

2.1 SYSTEM CONTROL AND MODE CONTROL BLOCK DIAGRAM FOR CLD-D703 AND CLD-D770

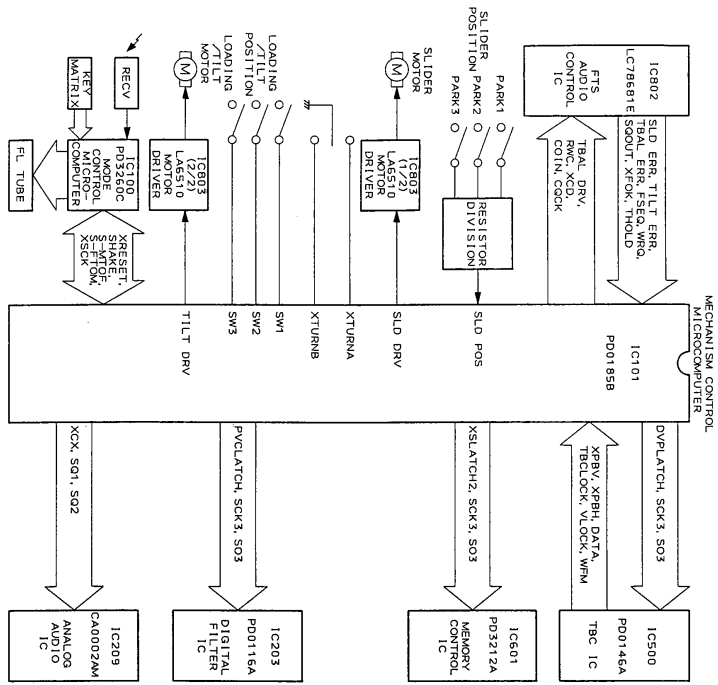


Fig. 2-1-1 SYSTEM CONTROL BLOCK DIAGRAM

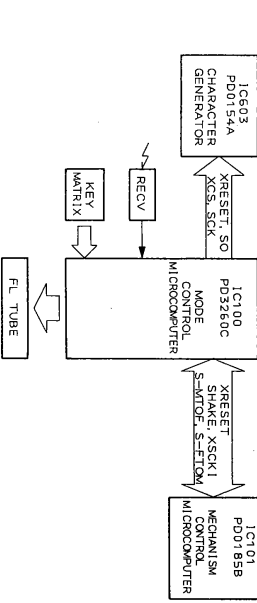


Fig. 2-1-2 MODE CONTROL BLOCK DIAGRAM

2.2 SYSTEM CONTROL BLOCK DIAGRAM FOR CLD-D503 AND CLD-D570

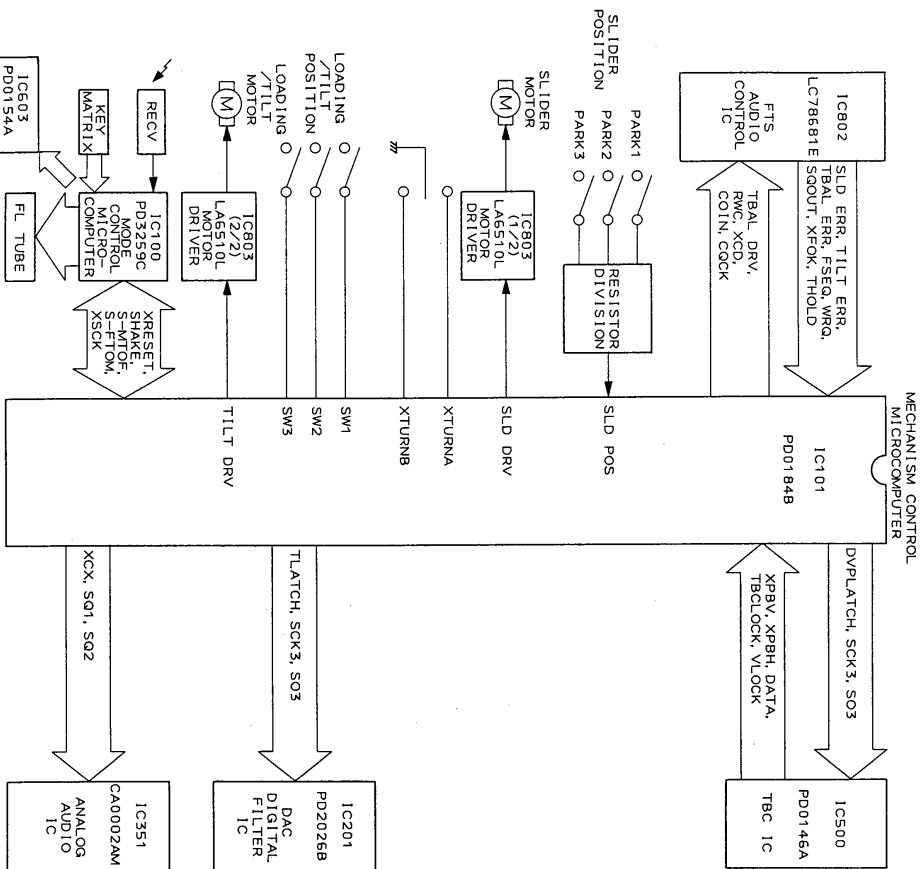


Fig. 2-2 SYSTEM CONTROL BLOCK DIAGRAM

2.3 SYSTEM CONTROL BLOCK DIAGRAM FOR CLD-S360

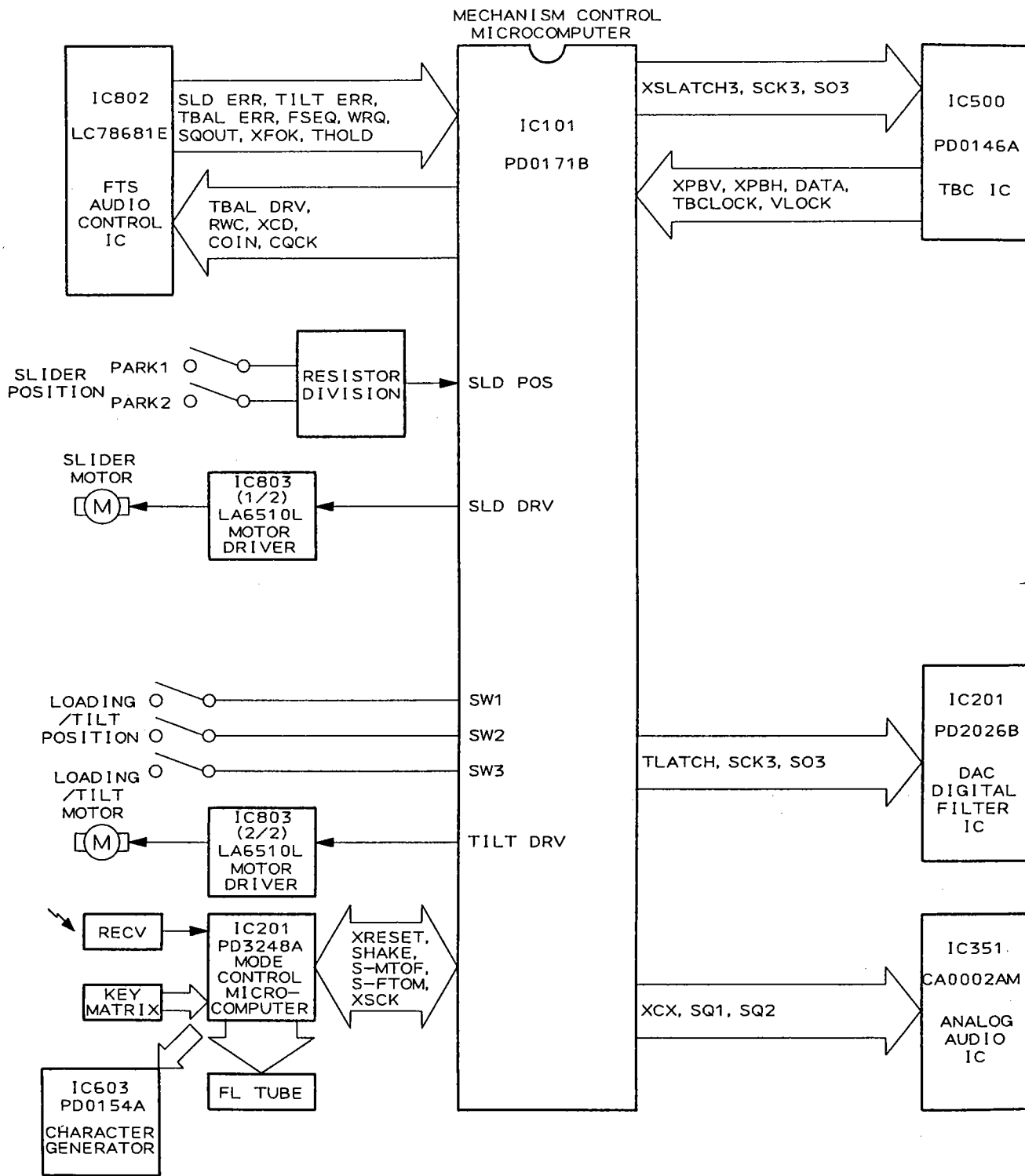


Fig. 2-3 SYSTEM CONTROL BLOCK DIAGRAM

2.4 INTERFACE BETWEEN MICROCOMPUTERS

This unit has an 8-bit microcomputer (IC101: refer to table 1) that controls the mechanism and an 8-bit microcomputer (IC100: refer to table 1) that controls operation/display. These two

microcomputers are connected by serial interface. This communication line also uses a character generator IC (IC603: PD0154A).

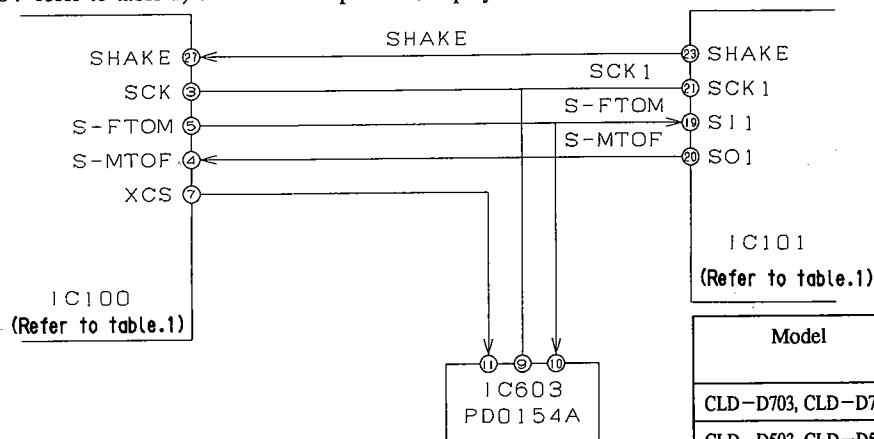


Fig. 2-4 Serial interface connection

Model	Mechanism control microcomputer	Mode control microcomputer
CLD-D703, CLD-D770	IC101 : PD0185B	IC100 : PD3260C
CLD-D503, CLD-D570	IC101 : PD0184B	IC100 : PD3259C
CLD-S360	IC101 : PD0171C	IC201 : PD3248A

Table 1: Mechanism Control Microcomputers and Mode Control Microcomputers

2.5 COMMUNICATION PROCEDURE BETWEEN MICROCOMPUTERS

For this explanation of the communications procedure between microcomputers, CLD-D703 is used as an example.

1. PD0185B sets SHAKE pin (23 pin) to several μ s "L" and requests PD3260C for commencement of communications.
2. Upon receiving request for commencement of communications, PD3260C sets SHAKE pin (27 pin) to "L" and informs PD0185B that communications is possible.
3. PD0185B switches SCK1 (21 pin), which it had been using as an input port, into output mode. PD3260C puts SCK (3 pin) into input mode and establishes communications line connection between microcomputers.
4. PD0185B sends out transmission clock (562.5kHz) at 8-bits and transmits each datum in synchronization with that clock.
5. When PD3260C receives 8-bit data, it sets SHAKE pin (27 pin) to "H" and signals that one communication has ended.

6. PD0185B puts SCK1 (21 pin) into input mode and PD3260C puts SCK (3 pin) into output mode and cuts off communications line to complete one communication.
- Communications is in 10-30ms cycles and 12-byte data can be transmitted at one time.
 - Handshake is done on one line and PD0185B and PD3260C use ports that are for both input and output. Output mode is in effect only when output is "L". At other times, input mode (high impedance) is in effect. Also, before output of "L", each confirms that SHAKE is "H" before carrying out operation. This prevents crosstalk of outputs.
 - To prevent transmission error when communicating data, a check code has been added. When transmission error has been detected 16 times continuously, PD3260C outputs a reset signal to PD0185B in order to return to the initial condition. Similar resetting is also done when communication of 300ms or more cannot be carried out.

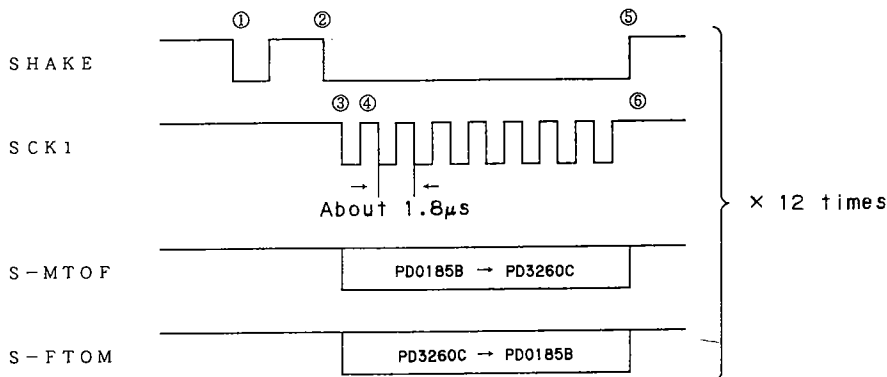


Fig. 2-5 Microcomputer-to-Microcomputer Timing Chart

2.6 OUTLINE OF MECHANISM CONTROL SYSTEM

1) Processing after power ON

After the power is turned on, reset is canceled (28 pin : L → H) and the mechanism control microcomputer (refer to table 1) carries out initialization in the following order.

1. Inside RAM and ports are initialized
2. Memory IC (IC601 : PD3212A) is initialized (CLD-D703, CLD-D770 only)
3. FTS-audio IC (IC802 : LC78681E) is initialized
4. Tray position is detected
5. Communications with mode control microcomputer (refer to table 1) is confirmed (If there is any abnormalities in communications, the following initialization steps are not carried out.)
6. TBC IC (IC500 : PD0146A) is initialized
7. Pickup position is initialized
8. Disc revolution is stopped
9. Loading mode is initialized

Normal operations are commenced after the above initialization procedures are completed.

2) Loading/tilt motor control

Loading/tilt motor drive is controlled by PWM signal output from the TILT DRV (refer to table 2) of the CONT section mechanism control IC(IC101) which goes through the OP amp (IC803). The voltage impressed on the loading/tilt motor is switched by the PWM signal duty as shown below. The PWM cycle is 30msec.

Model	TILT DRV pin
CLD-D703, CLD-D770	62
CLD-D503, CLD-D570	14
CLD-S360	14

Table 2: Mechanism Control IC TILT DRV Signal Output Pins

Motor operation		Duty (%)	PWM Signal waveform
Focus OFF	Stop	0	5.0V 2.5V 0V
	Loading	100	
	Unloading	Is changed to prevent feeling/overrun. refer to Fig. 2-6-2, 2-6-3.	
Focus ON	Large error	Tilt UP servo	
		Tilt DOWN servo	40
	Small error	Tilt UP servo	13 (CLD-S360 is 20)
		Tilt DOWN servo	20

Fig. 2-6-1

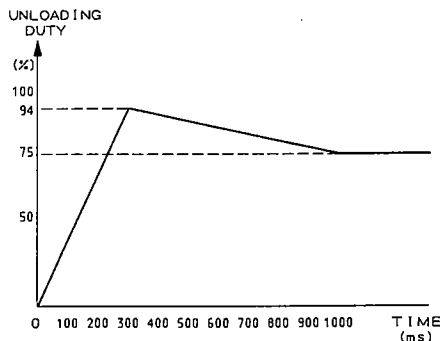


Fig. 2-6-2 Duty Changes at CLD-D503, CLD-D570, CLD-D703 and CLD-D770 Unloading

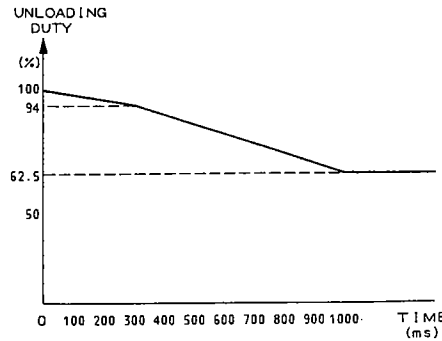


Fig. 2-6-3 Duty Changes at CLD-S360 Unloading

● Loading/clamping operation

When the tray is opened or closed and the disc is clamped or stopped, the motor operates while detecting the position of the cam gear with the loading/tilt position detection switch which is connected to SW1 - 3 of IC101 (refer to table 3).

● Tilt servo operation

Each time disc movement starts, the loading/tilt motor can be used for playing LD discs and CDV discs (video part) because of the tilt servo.

When the tilt servo is operating, the drive of the loading/tilt motor is PWM drive.

The tilt servo drives the loading/tilt motor so that the input voltage of TILT ERR of IC101 (refer to table 4) is 2.5V.

The ON/OFF conditions for the tilt servo are as shown below.

Model	SW1 - 3 pin
CLD-D703, CLD-D770	59-61
CLD-D503, CLD-D570	33-35
CLD-S360	33-35

Table 3 : Mechanism Control IC SW1 - 3 Output Pins

Model	TILT ERR pin
CLD-D703, CLD-D770	8
CLD-D503, CLD-D570	9
CLD-S360	9

Table 4 : Mechanism Control IC TILT ERR Input Pins

Disc part	Disc movement started	At normal play
LD	ON	All regions
CD,CDV audio part	ON	OFF
CDV video part	ON	0:00 - outer track 1:23 (disc with 3:00 or more recording) ON

Table 5 : Tilt Servo ON/OFF Conditions

When there is an abnormality in the disc or the tilt sensor circuit and input voltage of the TILT ERR pin does not enter the set range even if the pick up incline is more than +1.7 or -2.2 degrees, the mecha switch condition is detected and the loading motor's operation is stopped. The tilt servo switches the PWM duty between two steps according to the error value. When the error value is small (refer to table 6), the duty is small and when the error value is large (refer to table 6), the duty is large for PWM output. refer to Fig. 2-6-4.

Model	Error value is small	Error value is large
CLD-D703, CLD-D770	1.25V - 3.75V	0V - 1.25V, 3.75V - 5V
CLD-D503, CLD-D570	1.25V - 3.75V	0V - 1.25V, 3.75V - 5V
CLD-S360	0.625V - 4.375V	0V - 0.625V, 4.375V - 5V

Table 6 : Error Level Divisions

SW3	H	[Timing diagram: SW3 H is high from start to end]					
	L	[Timing diagram: SW3 L is low from start to end]					
SW2	H	[Timing diagram: SW2 H is high from start to end]					
	L	[Timing diagram: SW2 L is low from start to end]					
SW1	H	[Timing diagram: SW1 H is high from start to end]					
	L	[Timing diagram: SW1 L is low from start to end]					
HEX	6	4	5	1	0	2	3
Test mode indication	0	1	2	3	5	7	8
Position	Open	Loading	Stand-by	Clamp	Tilt -	Tilt +	Tilt limit

Fig. 2 - 6 - 4 Loading/Tilt Position

3) Slider Motor Control

Slider motor drive is controlled by PWM signal output from the SLD DRV pin 18 of the VSOP ASS'Y CONT section mechanism control IC (IC101) which goes through the OP amp (IC803). The voltage impressed on the slide tilt motor is switched by the PWM signal duty as shown below. The PWM cycle is approximately 910µsec.

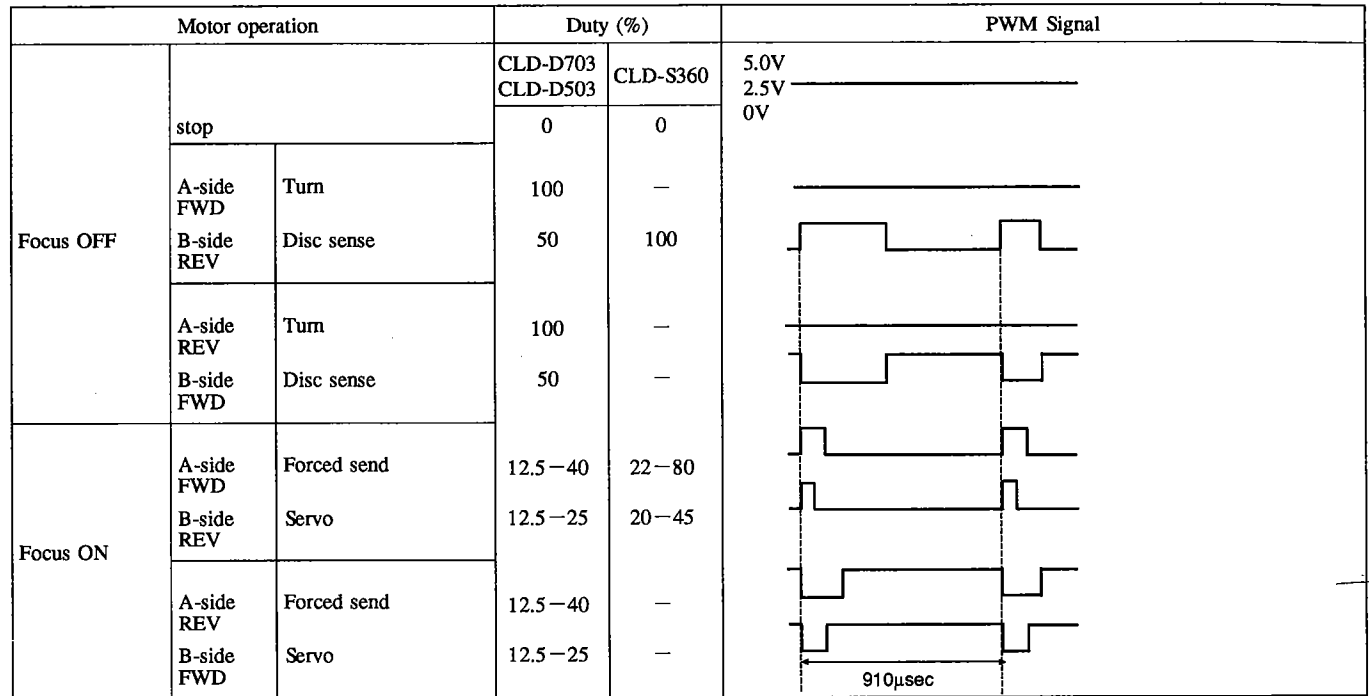


Fig. 2-6-5 Switching of Voltage Impressed on Slider Motor

The slider servo controls the slider motor so that the input voltage of the SLD ERR pin (refer to table 7) of the mechanism control IC is the same as the voltage at STOP.

Model	SLDR ERR pin
CLD-D703, CLD-D770	7
CLD-D503, CLD-D570	6
CLD-S360	6

Table 7: SLDR ERR Pins

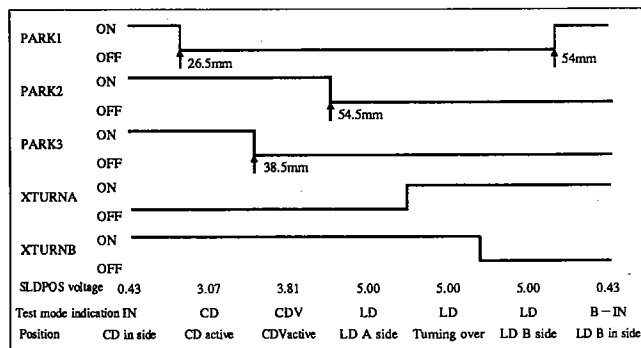


Fig. 2-6-6 Slider Position (CLD-D703, CLD-D770, CLD-D503 and CLD-D570)

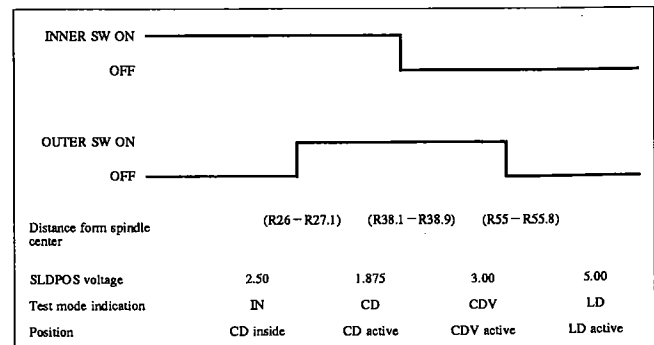


Fig. 2-6-7 Slider Position (CLD-S360)

4) Audio Control

XANA	SQ1	SQ2	Lch Line Out	Rch Line Out
L	L	L	Analog L channel	Analog R channel
	H	H	Mute	Mute
H	Following commands from microcomputer, LC78681E carries out switching between 3 conditions.		Digital L channel Digital L channel Digital R channel	Digital R channel Digital L channel Digital R channel

Fig. 2-6-8

At time of CD scan and LD clear scan (in case of digital sound selection), -12dB attenuated sound is output.

5) Clear Scan (CLD-D503, CLD-D570 and CLD-S360)

Through shuttling (main body: remote control), clear scanning without screen distortion can be carried out.

Depending on the angle that the shuttling is turned, it is possible to switch between color lock scan and clear scan. At time of clear scan, scan is carried out while outputting digital sound at -12dB (same as CD scan). (sound cannot be output when analog sound is selected.) The operation principles are given below.

1. In the clear scan mode, a prescribed number of tracks can be skipped with multi-track jumping.
2. In order to match phases of REF system and SG system, the mechanism control IC (refer to table 1) sends a shift enable command to the DVP IC (PD0146) and waits until the phases match (VLOCK="H").
3. Upon receiving the shift enable command, the DVP IC first eliminates phase difference between REF-H and SG-H by either decreasing or increasing SG-H at 6 clock increments. When there is no difference between H phases, the DVP IC eliminates phase difference between REF-V and SG-V by decreasing or increasing SG-V by 7H increments. When there is no phase difference, VLOCK is set to "H".
4. When VLOCK of the mechanism control IC becomes "H", squelch is canceled and the disc picture is shown for a fixed time. Step 1 is again returned to and steps 1 to 4 are repeated.

- * For sections where disc picture is not output, a black background is displayed.
- * During clear scan, the played digital sound is output in section where disc picture is output and in section that has VLOCK.
- * REF-H, V ... H-SYNC, V-SYNC of standard video signal
- * SG-H, V ... H-SYNC, V-SYNC generated by sync generator in DVP interior
- * VLOCK ... Signal that is emitted when H, V phases of REF system and SG system match.

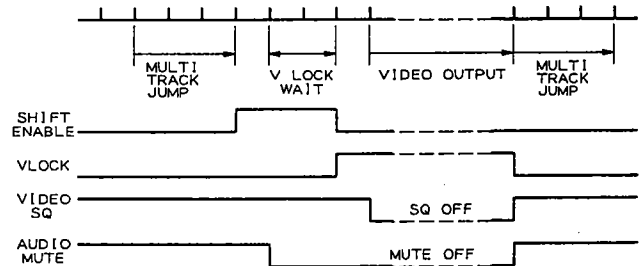


Fig. 2-6-9

● Clear Scan Timing Chart

CAV

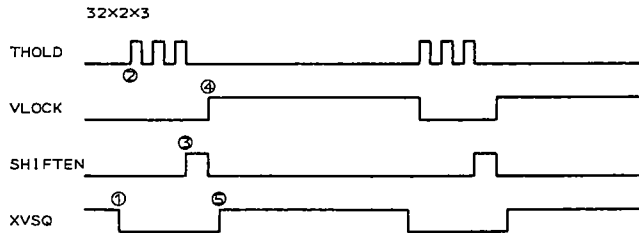


Fig. 2-6-10

- * SHIFT EN.XVSQ is serial command sent to DVP
- * The audio mute signal is put on at the same time as video squelch, but its cancellation is earlier than video squelch.

- ① : Video squelch is put on.
- ② : Multi-track jump $32 \times 2 \times 3$ is carried out.
- ③ : CLOCK, H decrease of increase is carried out to match phases of REF system and SG system. Shift enable (SHIFT EN) is ON.
- ④ : Since phases match (VLOCK="H")
- ⑤ : Video squelch is canceled and play is carried out for fixed time.

CLV : Compared with CAV, the time until phases are matched after jumping is long.

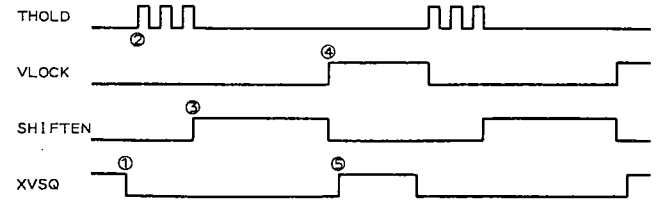


Fig. 2-6-11

● V-DNR (video digital noise reduction)

V-DNR is ON in at the following times :

- Normal play
- Strobe $\times 1$ FWD
- CAV/CLV multi-speed $\times 1$ FWD
- CAV still

However, V-DNR is OFF even at the following times :

- Test mode
- Video squelch ON

V-DNR can be changed with OFF, VARIABLE, and STANDARD buttons. In VARIABLE MODE, through shuttling, the NR amounts of Y (brightness) side and C (color) can be adjusted over ten steps. In variable mode, OFF and STANDARD are equivalent to no display (0) and middle value (5) respectively.

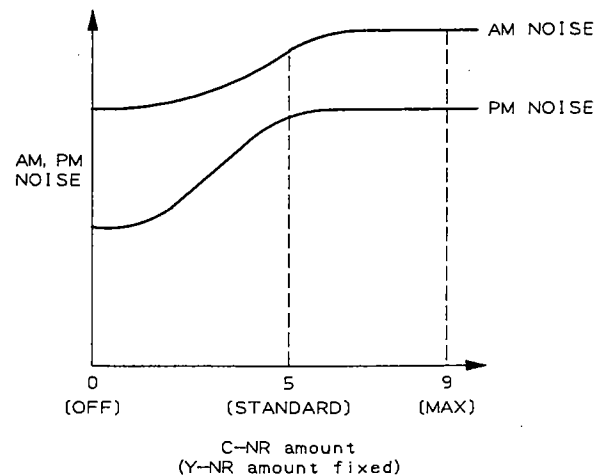
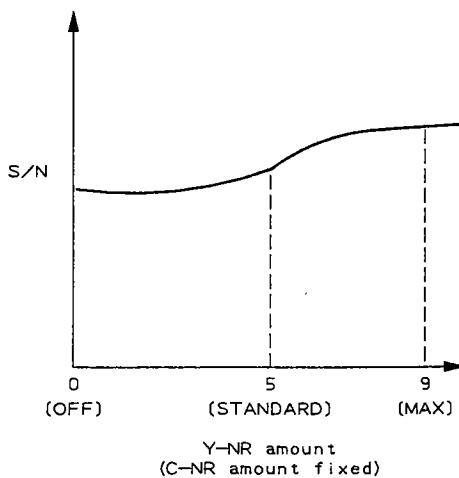


Fig. 2-6-12

6) Normal State Scan Timing Chart

●CLD -D703 and CLD -D770

With units that have video memory, four kinds of scan (×2, ×5, L SCAN, AND H SCAN) are possible by controlling the angle that the shuttle ring is turned.

CAV×2: Synchronization with play back V SYNC and multi-track jumping is carried out.

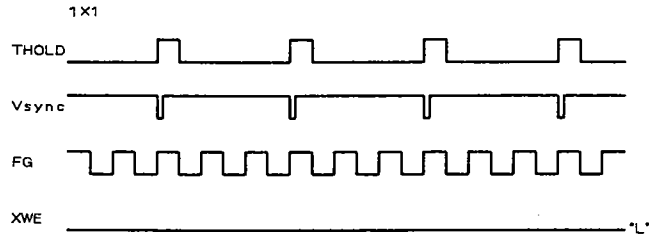


Fig. 2-6-13

* With XWE (X write enable), when the serial command to the memory control IC (PD0146) is "L", writing to memory is carried out, if it is "H", writing is stopped (freeze).

CAV×more than 2: FG is counted and multi-jumping is carried out for each revolution.

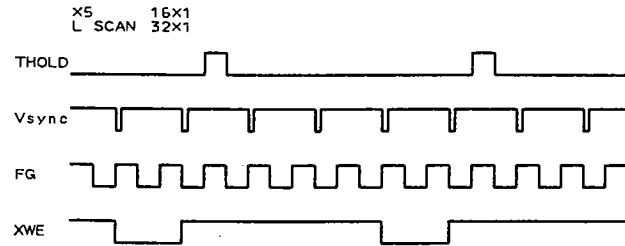


Fig. 2-6-14

CAV

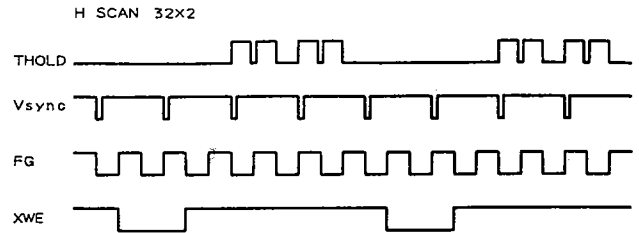


Fig. 2-6-15

CLV: FG is counted and multi-track jumping is carried out every four revolutions of inner track, three revolutions of middle track, and two revolutions of outer track.

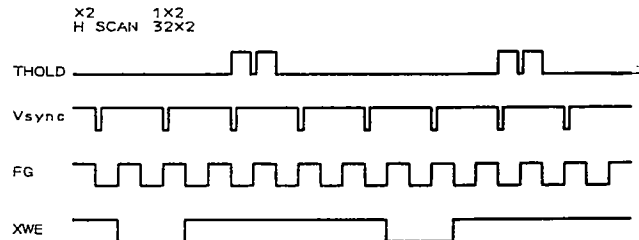


Fig. 2-6-16

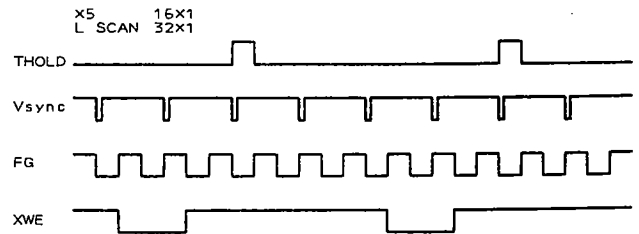


Fig. 2-6-17

●CLD -D503,CLD-D570 and CLD-S360

CAV: Synchronization with play back V SYNC and multi-track jumping is carried out.

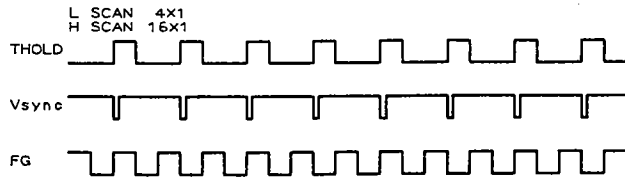


Fig. 2-6-18

CLV: FG is counted and multi-track jumping is carried out every four revolutions of inner track, three revolutions of middle track, and two revolutions of outer track.

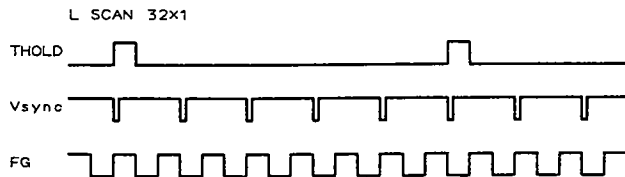


Fig. 2-6-19

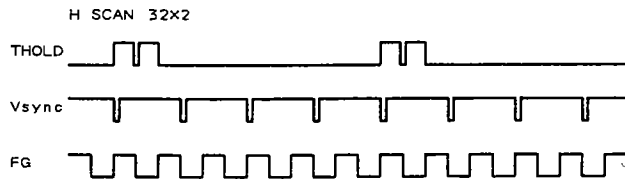


Fig. 2-6-20

7) Direct CD

At CD play, if the direct CD switch is turned on, the following operations are carried out. (Control by microcomputer)

- ①Self-lighting switch lights up and direct CD mode is entered.
- ②Power to video system portion that is unnecessary for CD play is turned OFF. (no indication)
- ③The slider park position is put into CD start position.
- ④When the tray is opened from its closed position, the small tray for CDs comes out.

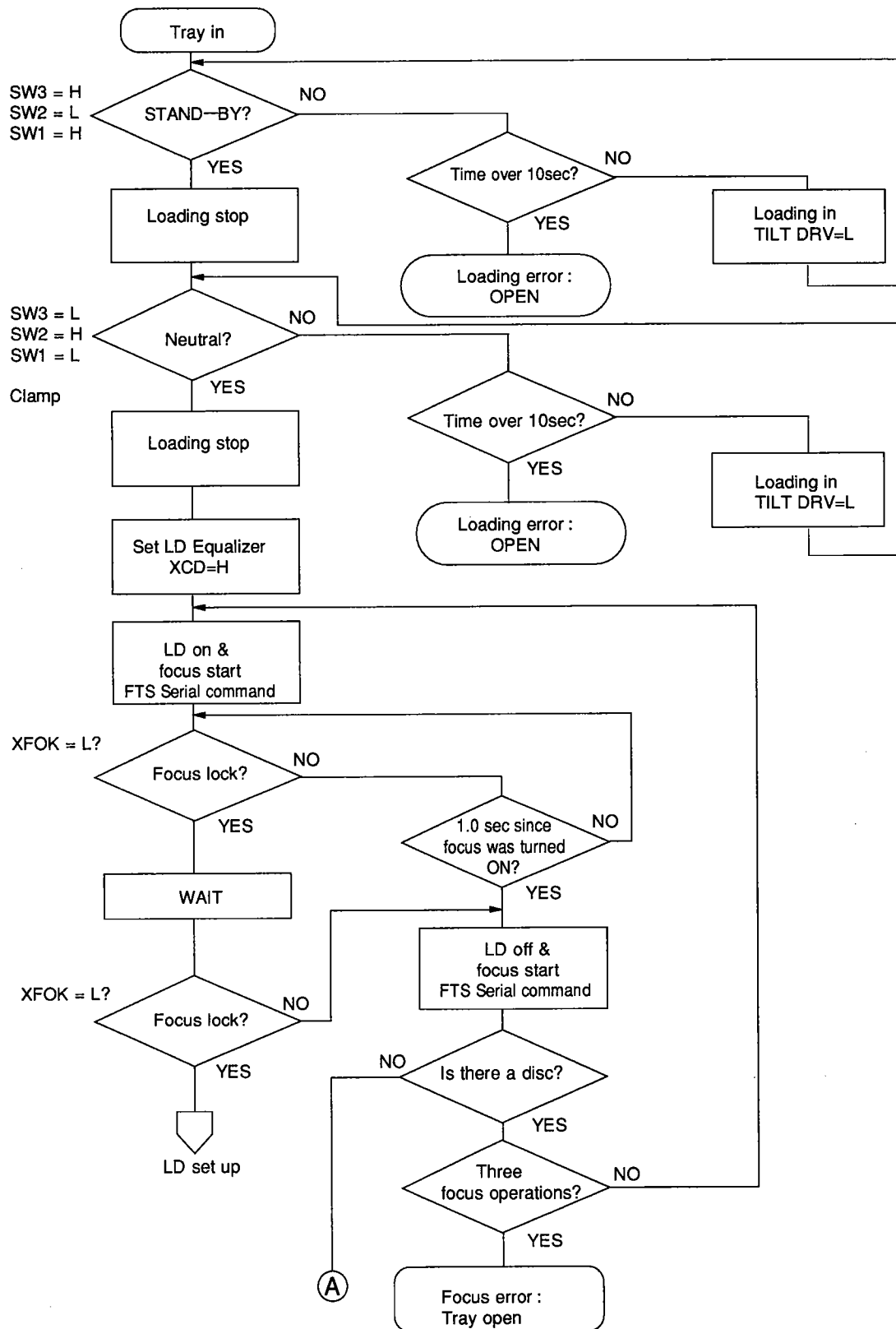
With these operations, the time its takes after play button is pushed until the CD is plays is 2/3. Also, because unnecessary power is cut off, more pure audio playing is possible.

If the direct CD switch is turned ON when the tray is open, the self-lighting switch will flash from the time the tray is closed until disc determination is finished. At the time that disc determination is finished, if there is a CD or CDV disc present or if there is no disc, the self-lighting switch is lit (flashing stops). If there is an LD, then it goes off and the CD mode is automatically canceled. Also, the direct CD switch cannot be turned ON during LD play.

If a CDV disc is played, when the video part is played, the video system's power will go on temporarily, but the direct CD mode is not canceled. When video part play is finished, the normal direct CD mode is returned to.

2.7 FLOW CHART OF EACH OPERATION

1) From Tray Open to Tray-In Flow Chart

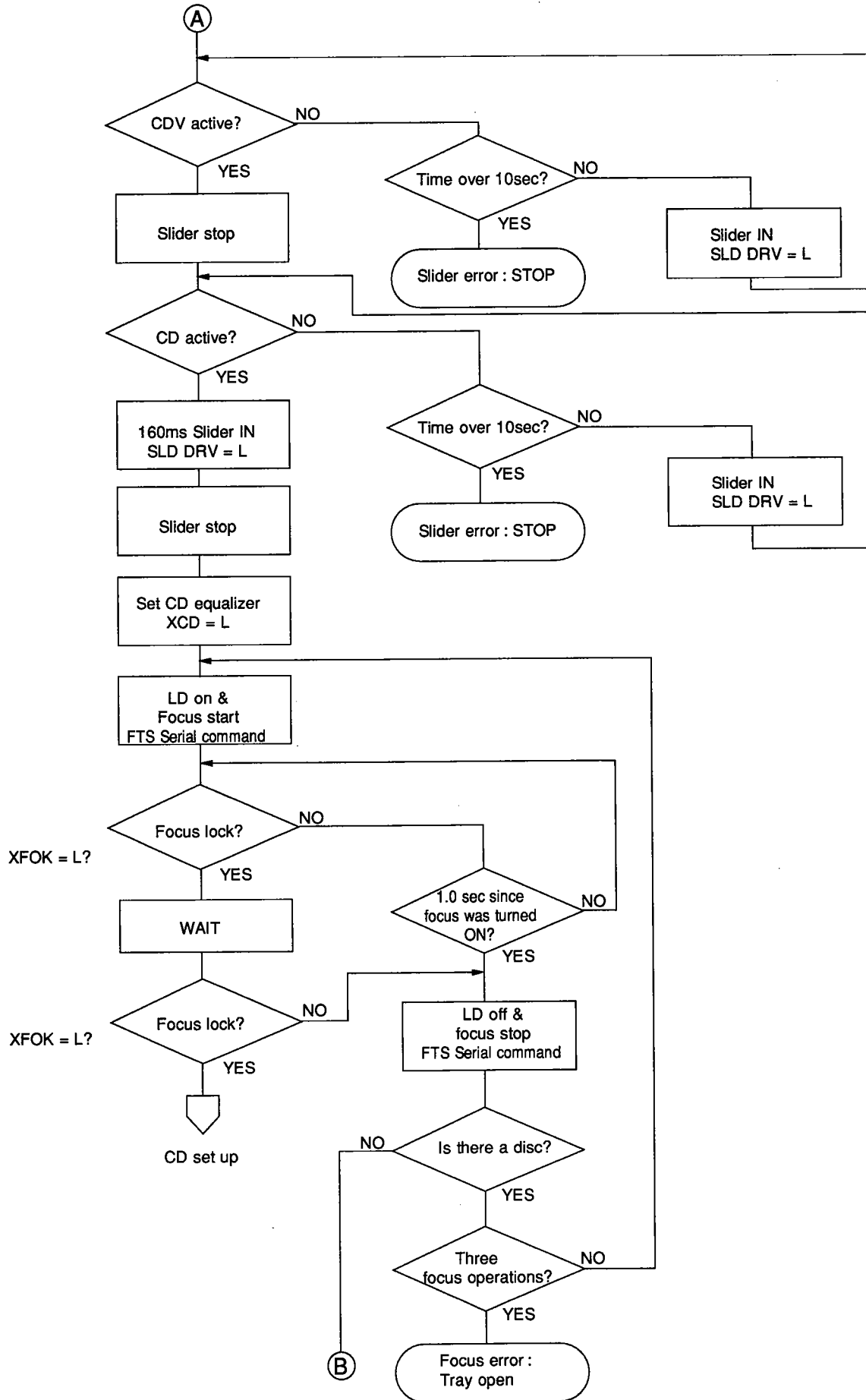


From tray open state to completion of tray-in.

If loading operation is not finished within 10 seconds, the situation is judged as abnormal and the tray is opened.

When there is a disc and focus does not lock even after three focus sweeps, the situation is judged as abnormal and the tray is opened.

Fig. 2-7-1



Slider operation is stopped if it is not completed within a fixed time. After that, only OPEN key will evoke response.

Fig. 2-7-2

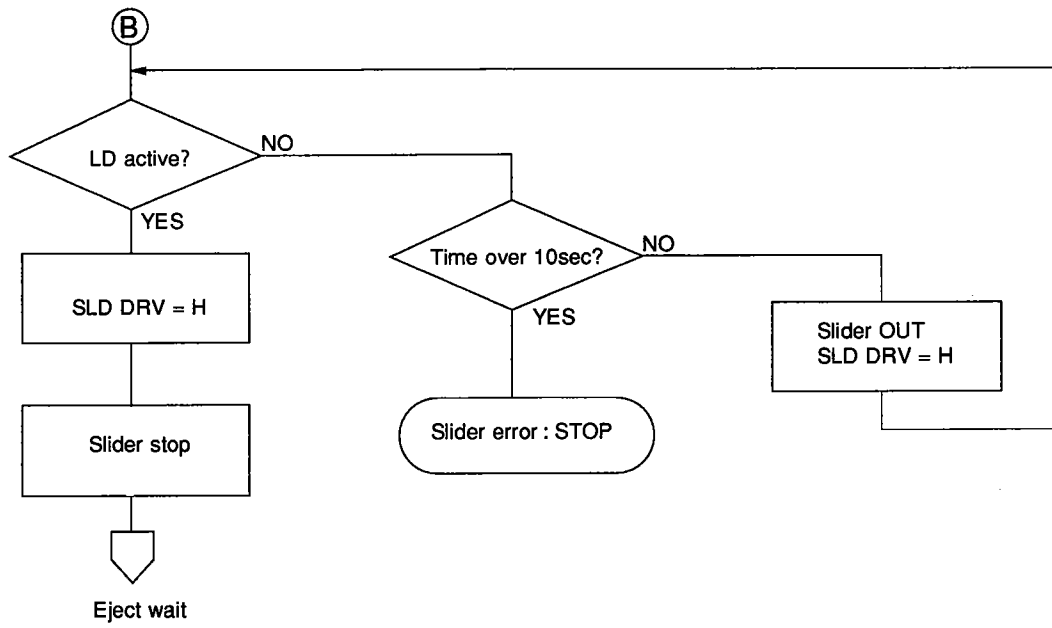
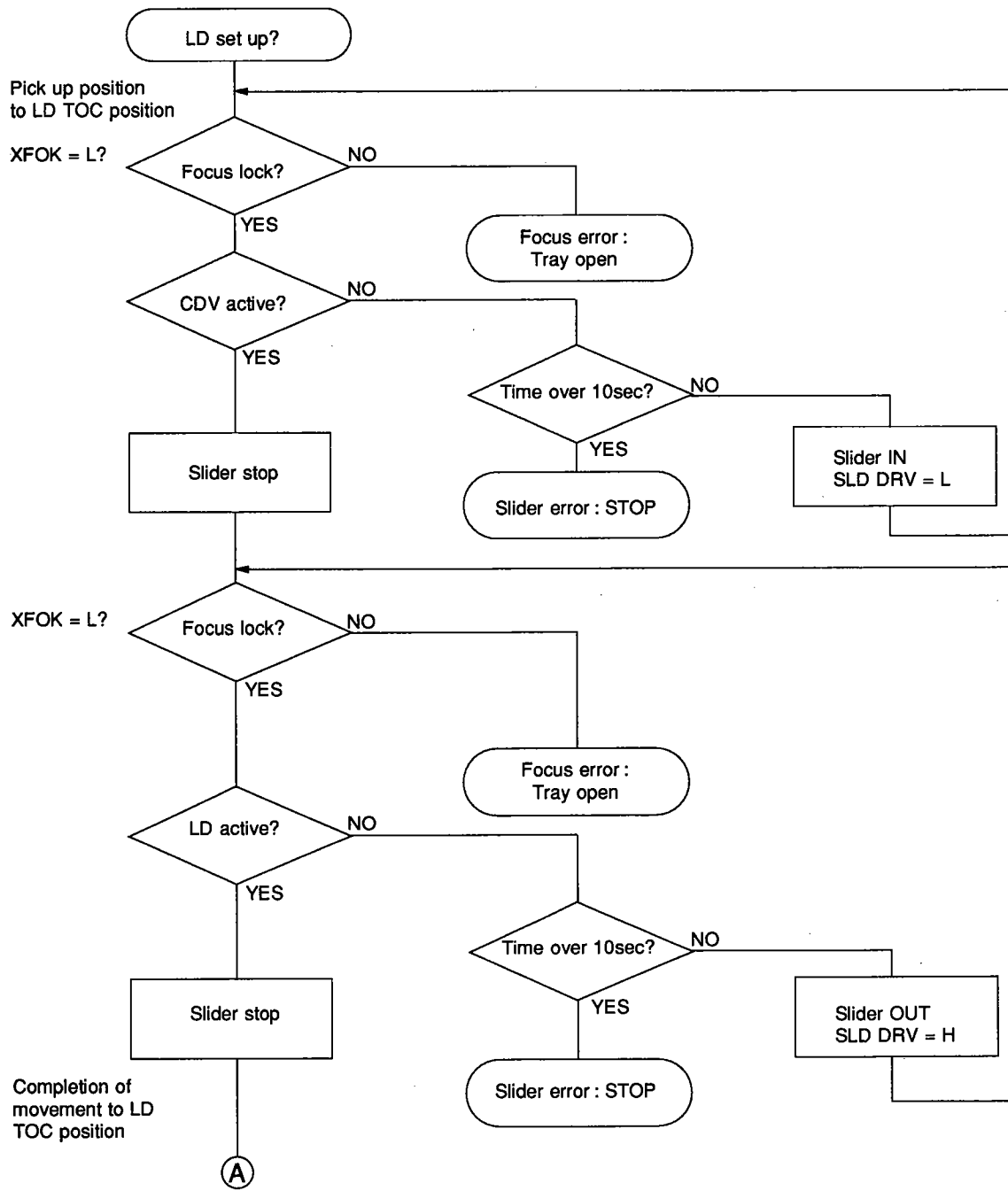


Fig. 2-7-3

2) LD Set-up Flow Chart



• During movement to spindle start position, if the focus is cannot be achieved, it is determined that there are overlapping LD, CD and the tray is opened.

Fig. 2-7-4

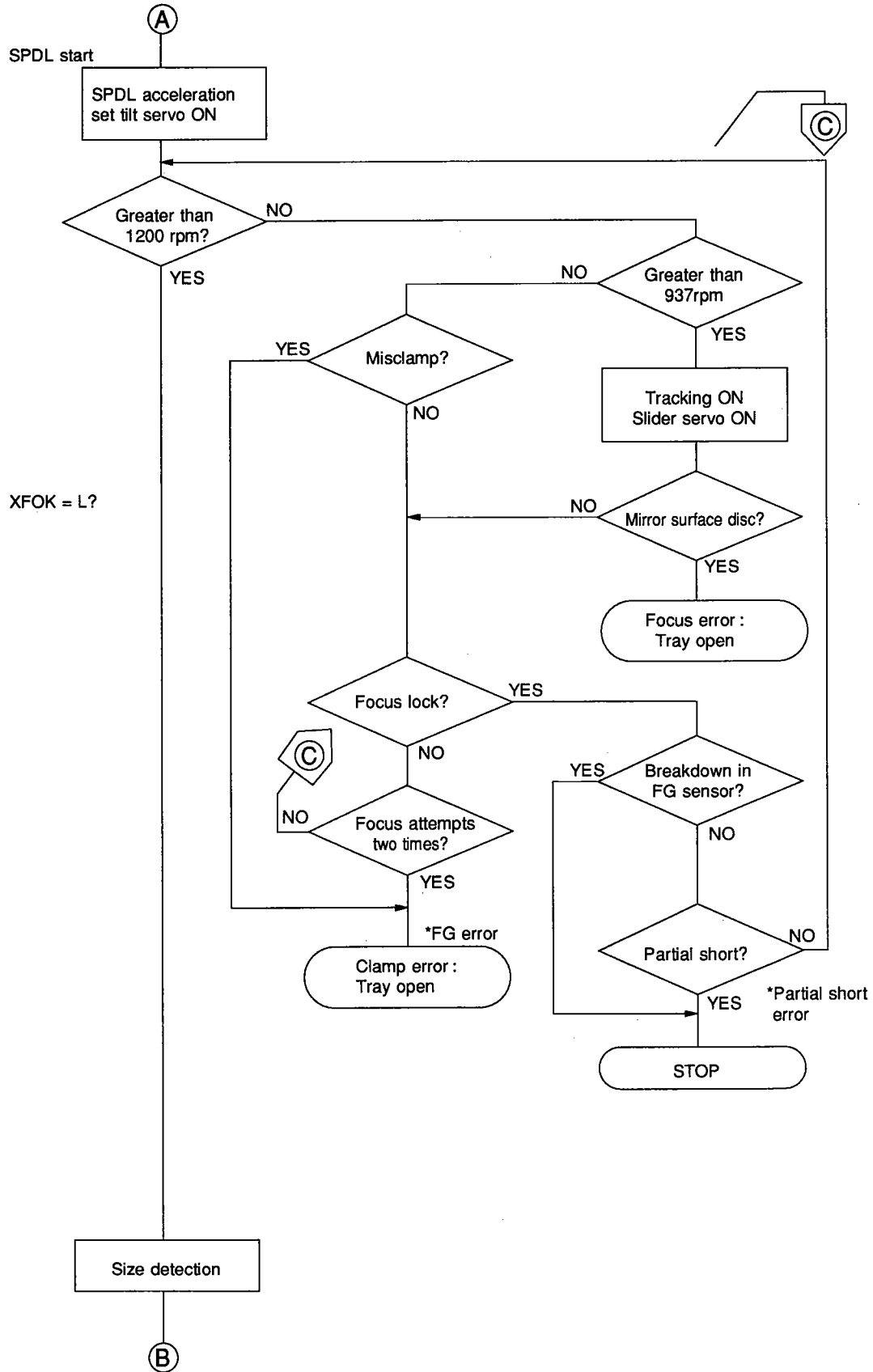


Fig. 2-7-5

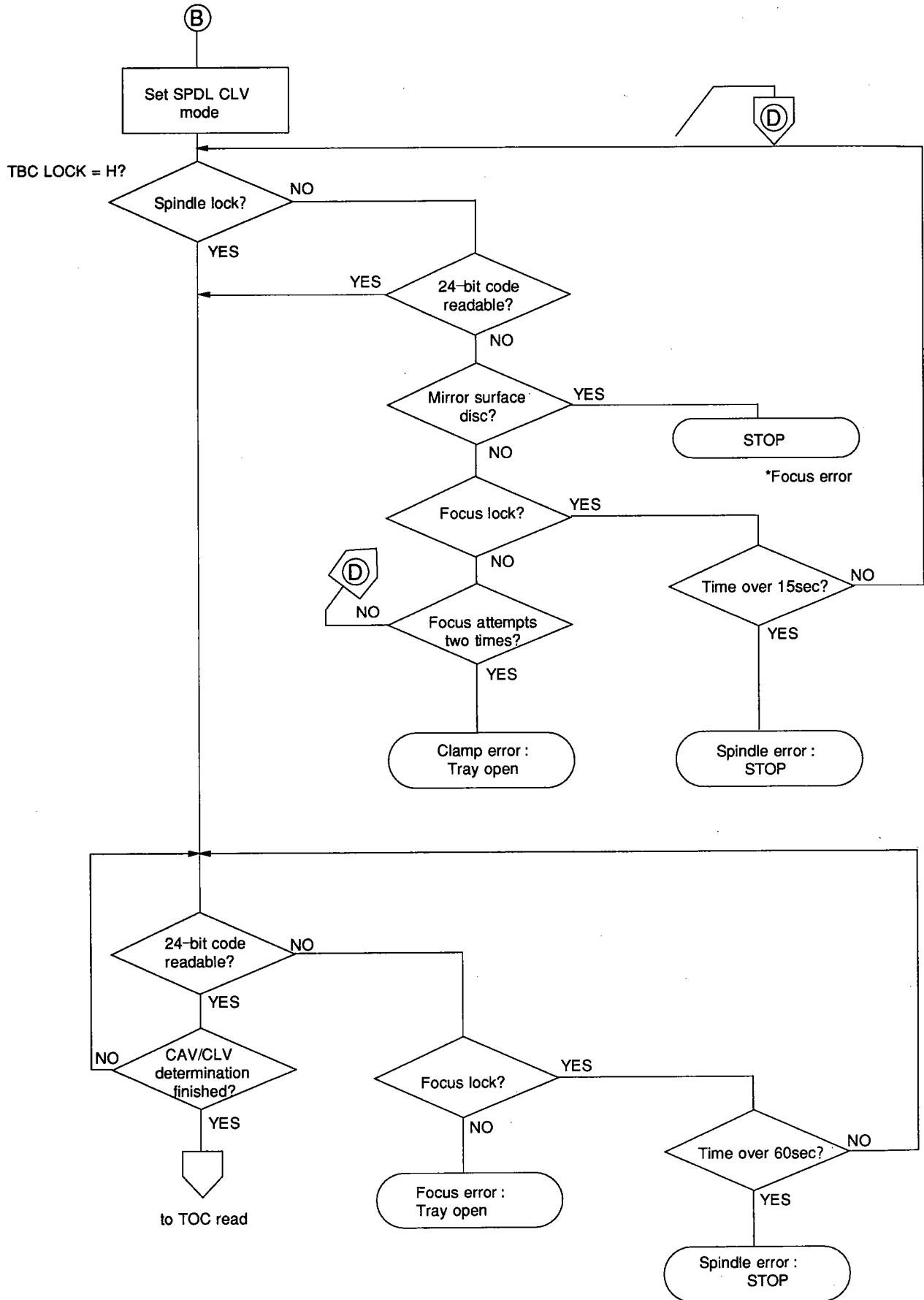
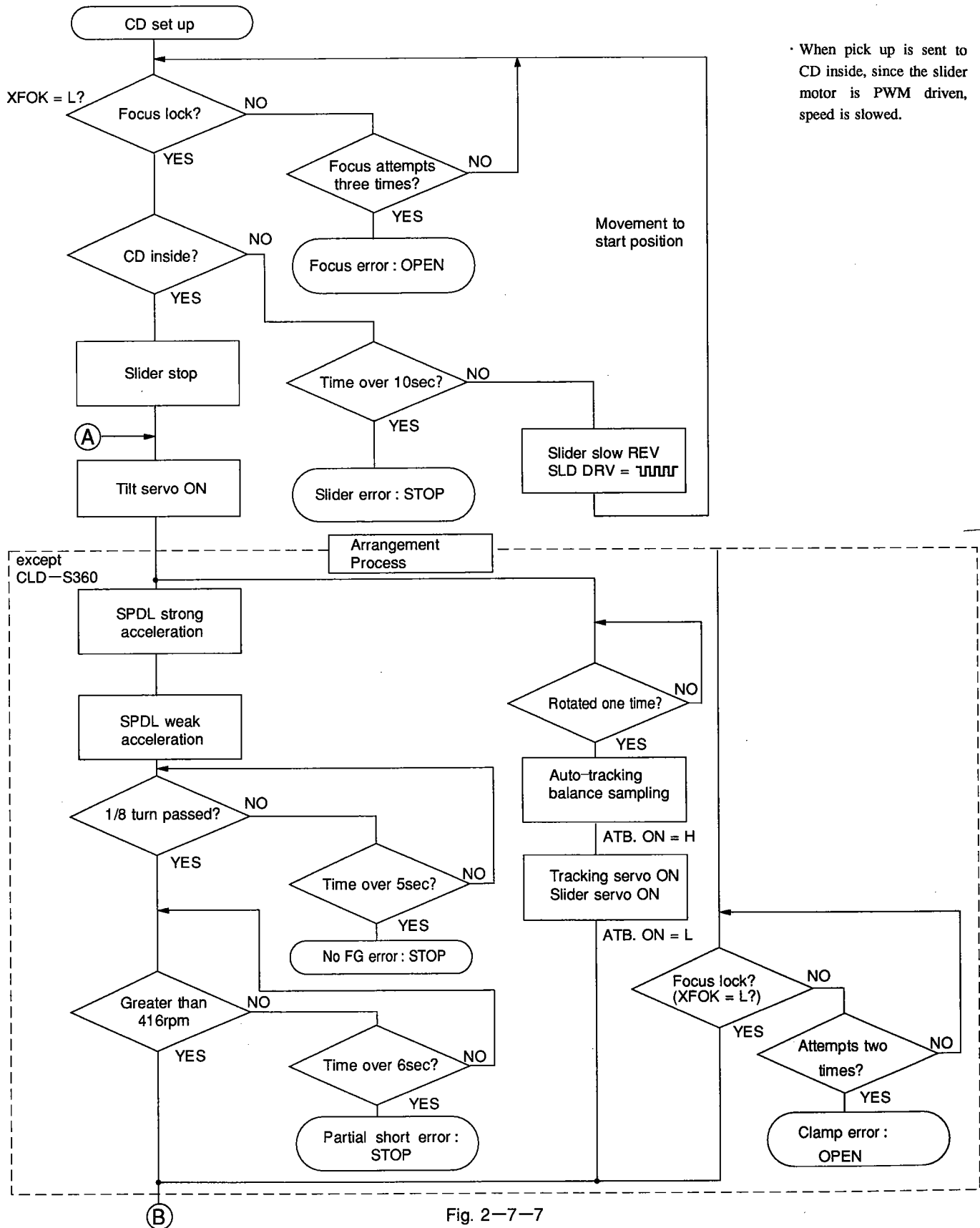


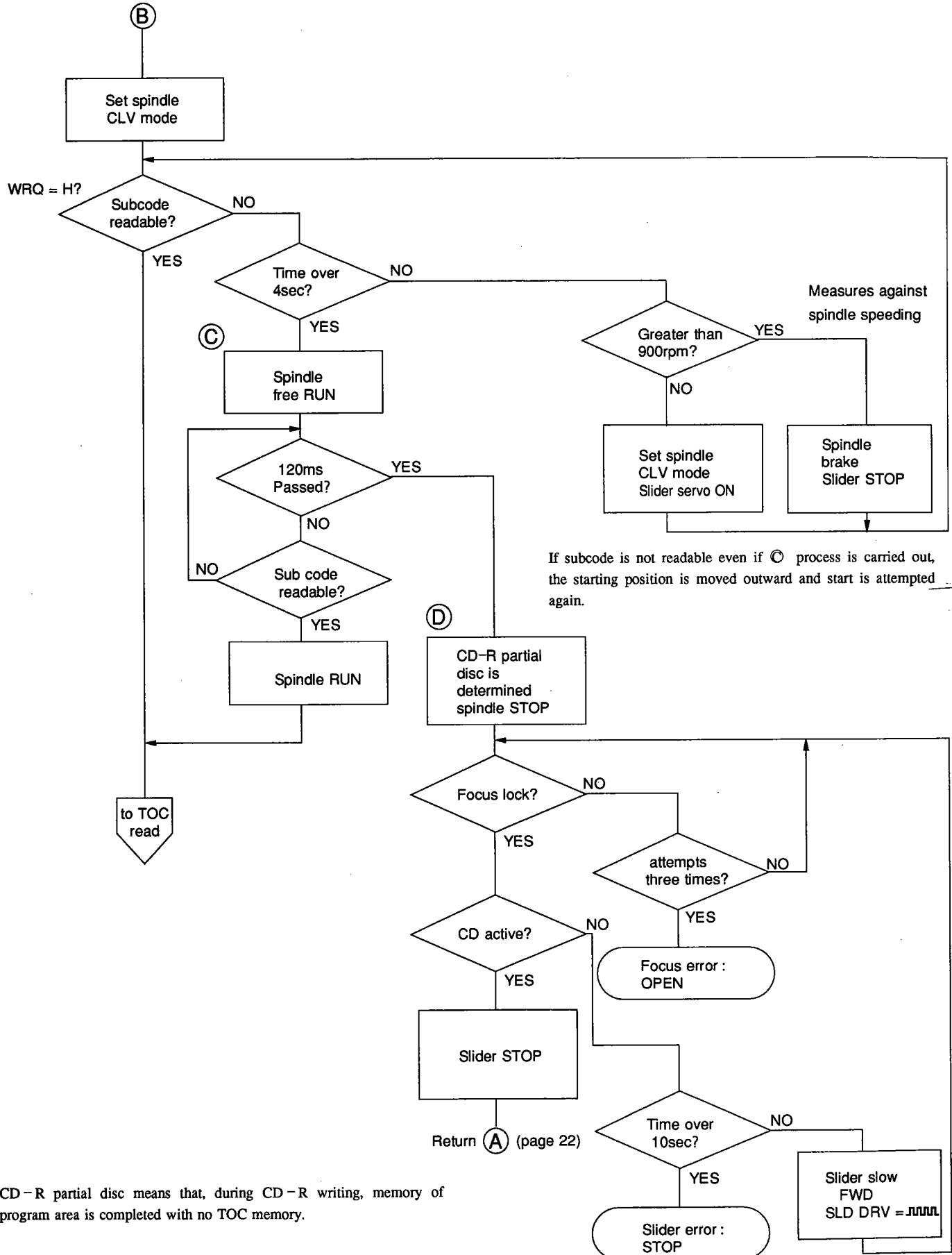
Fig. 2-7-6

3) CD Set Up Flow Chart



When pick up is sent to CD inside, since the slider motor is PWM driven, speed is slowed.

Fig. 2-7-7



• CD-R partial disc means that, during CD-R writing, memory of program area is completed with no TOC memory.

Fig. 2-7-8

4) Disc Search for CLV, CAV Discs Without TOC Flow Chart

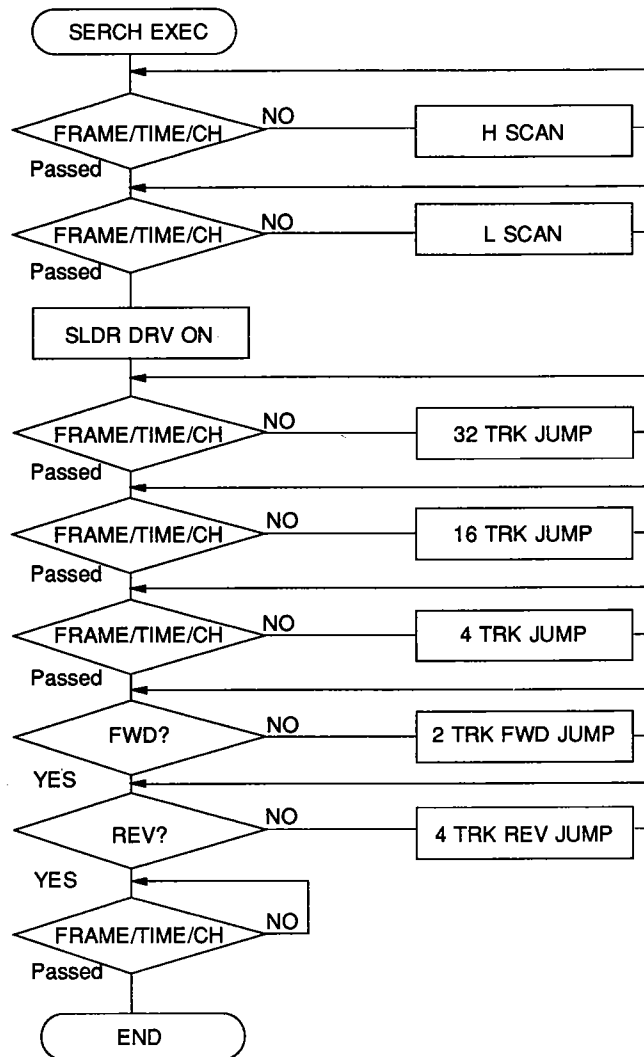


Fig. 2-7-9

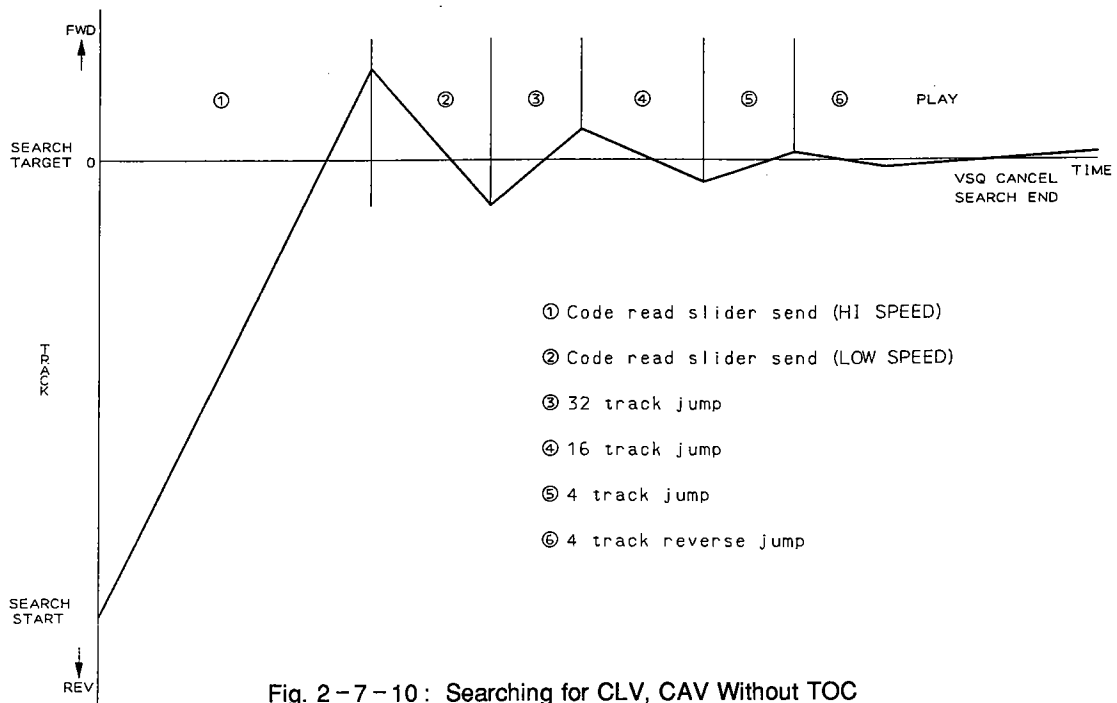


Fig. 2-7-10: Searching for CLV, CAV Without TOC

5) Disc Search for CLV With TOC Flow Cart

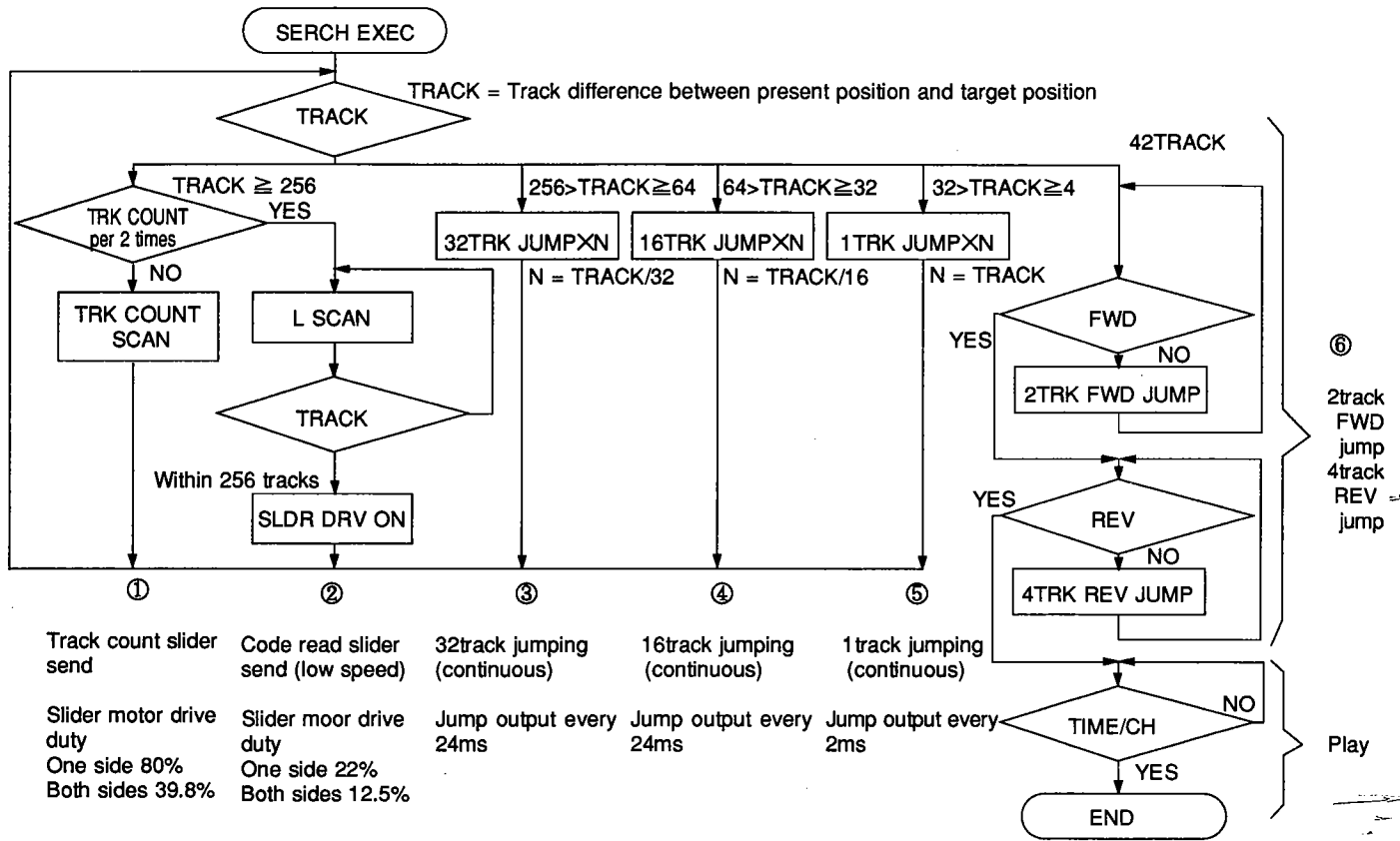


Fig. 2-7-11

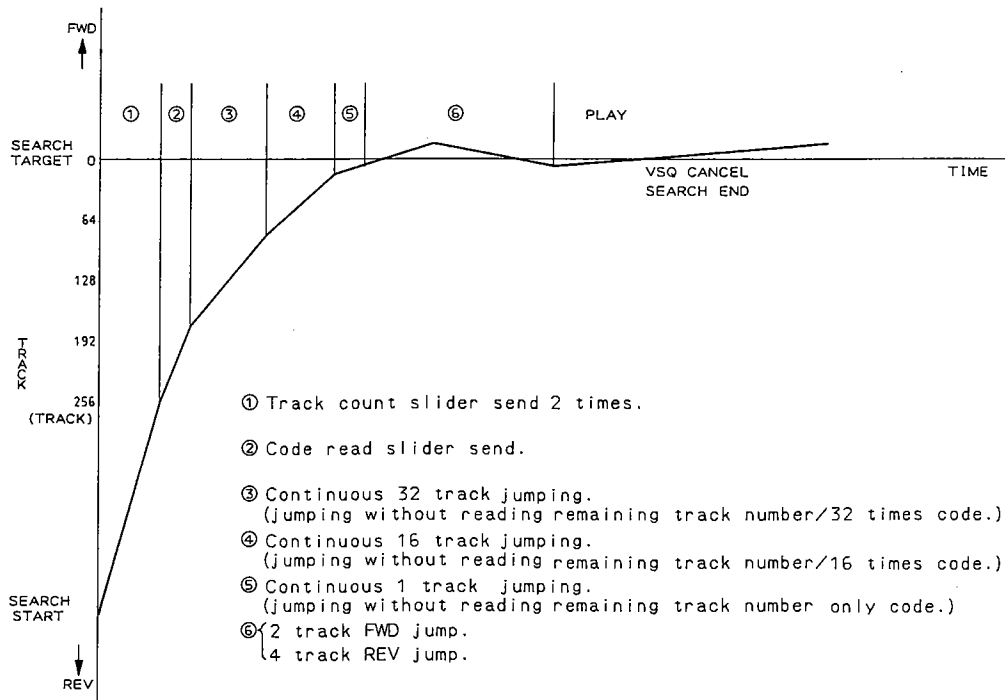


Fig. 2-7-12 Search for CLV with TOC

6) Turning from Side A to Side B (except CLD—S360)

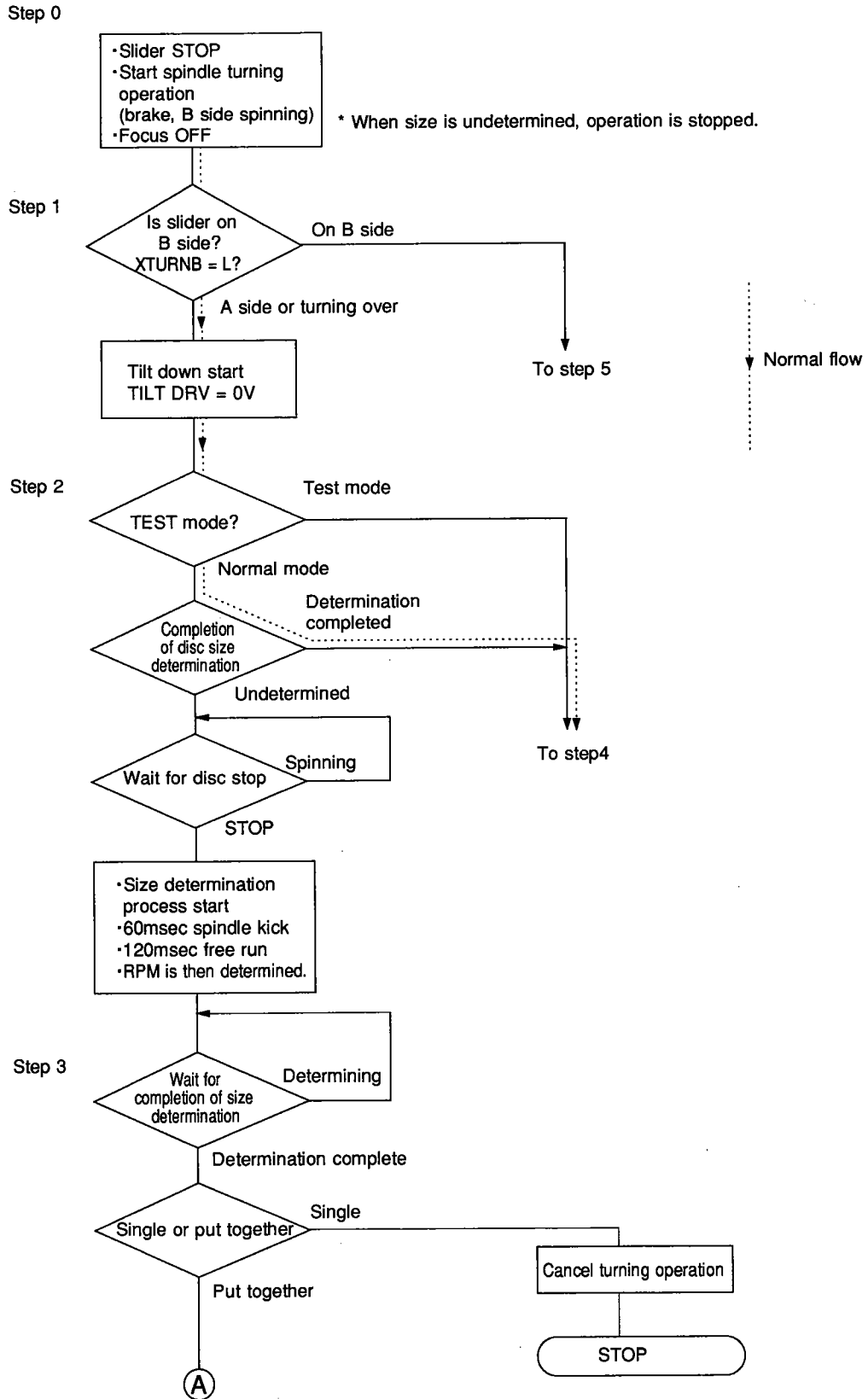
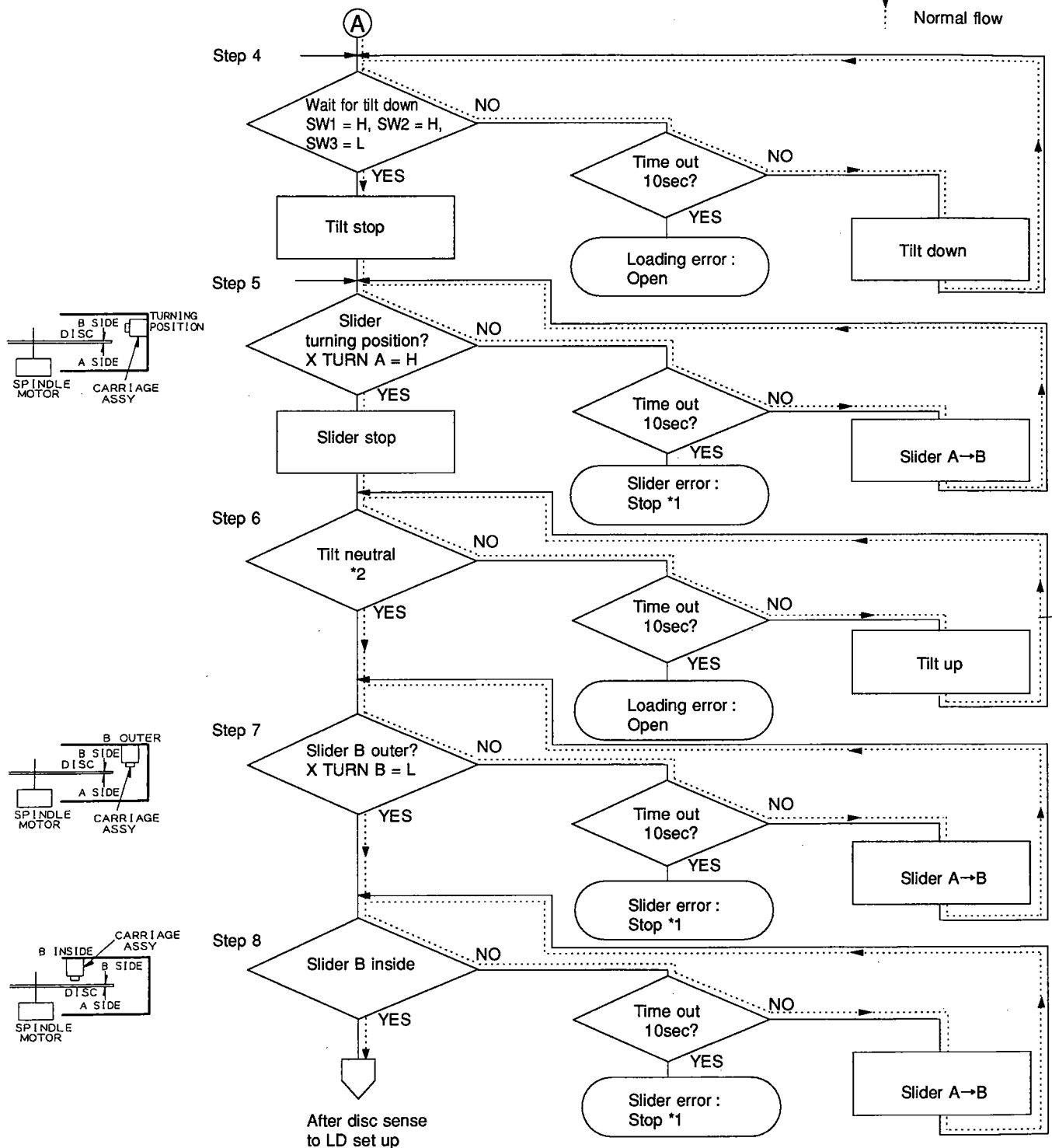


Fig. 2-7-13



* 1 : If there is slider error, only open and power keys will evoke response. In this condition, if the power key is pressed, the power will immediately go off.

* 2 : Tilt neutral is the position of the slider when it is shifted in the down direction until tilt plus (SW1 = L, SW2 = H, SW3 = L) is reached after having been moved in up direction until tilt minus (SW1 = L, SW2 = L, SW3 = L) is reached.

Fig. 2-7-14

7) Turning from Side B to Side A (except CLD-S360)

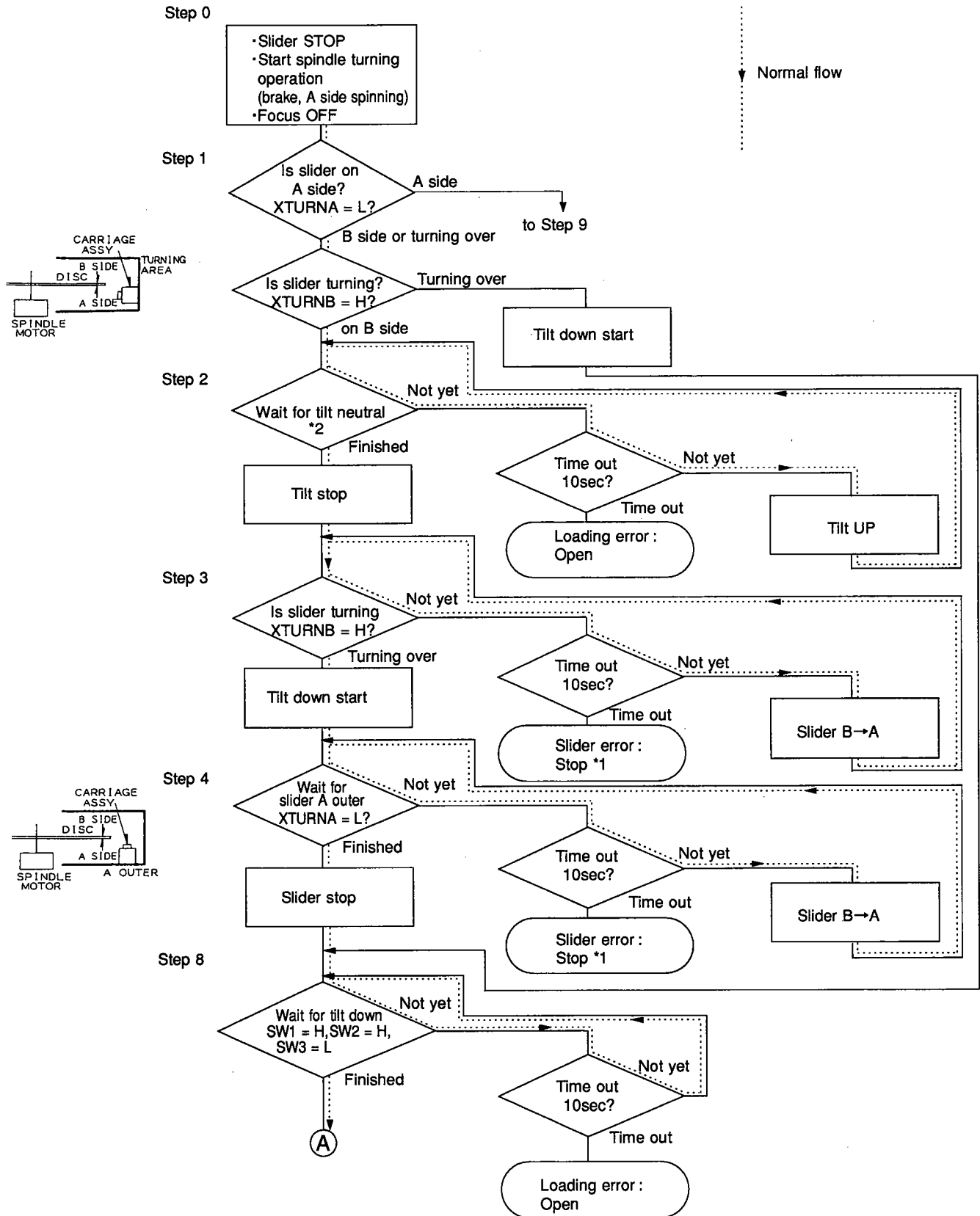
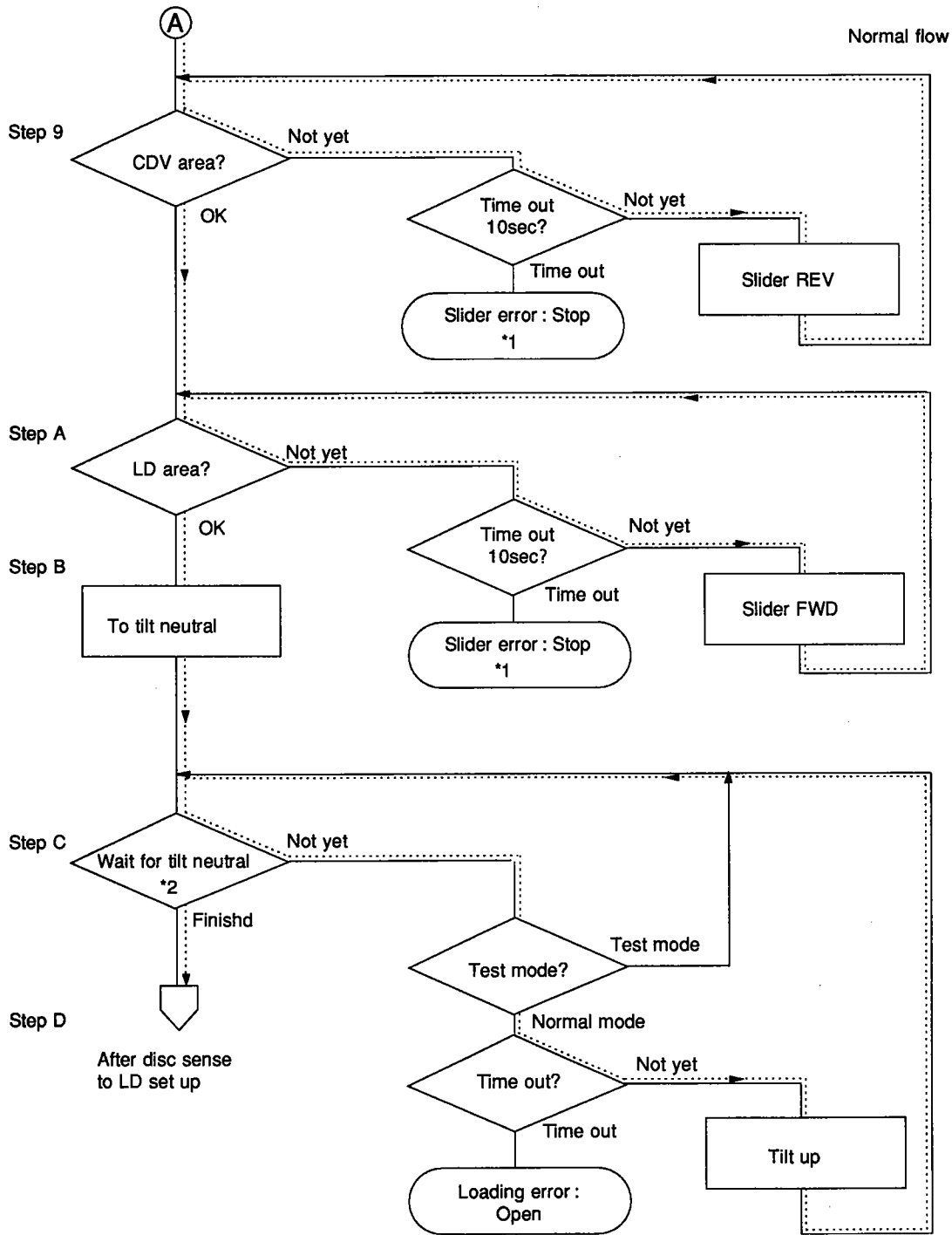


Fig. 2-7-15



* 1 : If there is slider error, only open and power keys will evoke response. In this condition, if the power key is pressed, the power will immediately go off.

* 2 : Tilt neutral is the position of the slider when it is shifted in the down direction until tilt plus (SW1 = L, SW2 = H, SW3 = L) is reached after having been moved in up direction until one degree tilt minus (SW1 = L, SW2 = L, SW3 = L) is reached.

Fig. 2-7-16

2.8 TABLE OF OPERATION MODES

●except CLD—S360

(1) Mecha mode = 1 open mode

Mecha step	Description
0	open entry
1	side change check, disc status clear
2	wait for tilt neutral, set slider to A-side outer track
3	tilt down set
4	wait for slider movement
5	dummy
6	dummy
7	dummy
8	wait for loading motor operation finish
9	move slider to home position
A	wait for slider movement
B	spindle check
C	loading to unload
D	wait for loading motor operation finish
E	100ms timer set
F	wait for timer
10	loading to open
11	mecha mode all end

(2) Mecha mode = 2 standby mode

Mecha step	Description
0	stop entry
1	side change check, disc status clear
2	wait for tilt neutral, set slider to A-side outer track
3	tilt down set
4	wait for slider movement
5	dummy
6	dummy
7	dummy
8	wait for loading motor operation finish
9	move slider to home position
A	wait for slider movement
B	spindle check
C	set loading mode to standby or vertical movement
D	wait for loading motor operation finish
E	mecha mode all end

(3) Mecha mode = 3 stop mode

Mecha step	Description
0	stop entry
1	side change check, disc status clear
2	wait for tilt neutral, set slider to A-side outer track
3	tilt down set
4	wait for slider movement
5	dummy
6	dummy
7	dummy
8	wait for loading motor operation finish
9	move slider to home position
A	wait for slider movement
B	spindle check
C	tilt neutral set
D	wait for loading motor clamp finish
E	mecha mode all end

(4) Mecha mode = 4 disc sense mode

Mecha Step	Description
0	if B-side, to step F if CD or CDV, to step 4
1	LD EQ setting, CAV setting, slider target setting
2	wait for slider movement (LD sense position)
3	wait for focus lock, when locked, confirm LD and go to mecha mode all end
4	wait for focus OFF
5	LD fix or if B-side go to step B, CD EQ setting, slider target setting
6	wait for slider movement (CD sense position)
7	wait for focus lock, when locked, confirm CD and go to mecha mode all end
8	wait for focus OFF
9	LD EQ setting, CAV setting, slider target setting
A	wait for slider movement (LD sense position)
B	if there is no CD direct, go to step E
C	wait for focus lock, when locked, confirm LD and go to mecha mode all end
D	wait for focus OFF
E	set to no disc and go to mecha mode all end
F	slider target setting, if single is confirmed, go to step 13
10	wait for slider movement (B side inside position)
11	wait for focus lock, when locked, confirm LD and go to mecha mode all end
12	wait for focus OFF
13	set to no disc and go to mecha mode all end

(5) Mecha mode = 5 set up mode

Mecha Step	Description
0	slider target setting
1	wait for slider movement (TOC position)
2	spindle start
3	wait for spindle lock, check for LD mis-clamp also carried out
4	check for PRD or mis-lock
5	with LD if in read in, read out area, go to step 6 anything else go to step 7
6	after moving slider to program area, go to step 5
7	play mode entry

(6) Mecha mode = 6 TOC read mode

Mecha Step	Description
0	TOC entry
1	read in search (slider REV sending)
2	program area search (16-track forward jump)
3	read in search (4-track REV jump)
4	wait for program area with play
5	reading 1st time TNO address
6	wait for spindle lock
7	jump back
8	if TOC cannot be read, treat as LD without TOC and go to mecha mode all end
9	1st time initialize to 0 15 second timer setting
A	wait for TOC reading with read in if readable, end if program area, go to next
B	if subcode is readable, 32-track REV jump
C	if subcode is readable, 32-track REV jump
D	if subcode is readable, 32-track REV jump
E	if subcode is readable, 32-track REV jump
F	return to step A
10	set PRD flag, start movement to program area
11	movement play to program area, 15 second timer setting
12	REV × 8 jump from TNO = 0 to IX = 0 generate code error and end

(7) Mecha mode = 7 play mode

Mecha Step	Description
0	play mode entry

(8) Mecha mode = 8 search mode

Mecha Step	Description
0	search mode entry
1	area change (A/V change)
2	area change wait timer setting
3	wait for area change
4	TOC check & TOC data setting
5	track count slider send entry
6	wait for track count slider send
7	wait for tracking error convergence
8	code read slider send (high speed)
9	code read slider send (low speed)
A	wait for tracking error convergence
B	256 track count slider send entry
C	256 track count slider send waiting
D	wait for tracking error convergence
E	32-track continuous jumping
F	wait for end of 32-track continuous jumping
10	16-track continuous jumping
11	wait for end of 16-track continuous jumping
12	1-track continuous jumping
13	wait for end of 1-track continuous jumping
14	32-track jumping
15	16-track jumping
16	4-track jumping
17	jump until right before target
18	play until target
19	search error processing when search time limit is passed
1A	when a new target is given during search

(9) Mecha mode = 9 side A → B mode

Mecha Step	Description
0	stop mode entry
1	side change convert from A-side mode to B-side mode
2	size determination (8" single or other)
3	wait for size determination end
4	wait for tilt down, set slider to B-side
5	tilt neutral set
6	wait for loading motor operation end
7	wait for slider movement
8	slider target setting (B-side inside)
9	wait for slider movement
A	mecha mode all end

(10) Mecha mode = A side B → A mode

Mecha step	Description
0	stop entry
1	side change check, disc status clear
2	wait for tilt neutral, set slider to A-side outer track
3	tilt down set
4	wait for slider movement
5	dummy
6	dummy
7	dummy
8	wait for loading motor operation finish
9	move slider to home position
A	wait for slider movement
B	tilt neutral set
C	wait for loading motor clamp finish
D	mecha mode all end

(11) Mecha mode = E power off mode

Mecha step	Description
0	stop entry
1	side change check, disc status clear
2	wait for tilt neutral, set slider to A-side outer track
3	tilt down set
4	wait for slider movement
5	dummy
6	dummy
7	dummy
8	wait for loading motor operation finish
9	move slider to home position
A	wait for slider movement
B	spindle check
C	power off check
D	wait for loading motor clamp finish
E	mecha mode all end

(12) Mecha mode = F recover mode

Mecha Step	Description
0	recover entry & slider movement
1	spindle hold
2	wait for spindle lock
3	spindle stop & slider movement
4	spindle stop & slider movement
5	wait for spindle lock end
6	turn slider movement direction
7	timer setting
8	wait for timer & focus lock check
9	wait for timer & slider movement
A	wait for spindle lock
B	recover error
C	CD/CDV recover mode
D	wait for spindle lock
E	recover error

Table of mecha mode

●CLD—S360 only

(1) Mecha mode = 1 open mode

Mecha step	Description
0	open entry
1	side change check, disc status clear
2	wait for tilt up
3	spindle check
4	wait for slider movement
5	switching the clamp to A-side
6	wait for loading motor operation finish
7	tilt down setting
8	wait for loading motor operation finish
9	move slider to home position
A	spindle check
B	wait for slider movement
C	loading to unload
D	wait for loading motor operation finish
E	100ms timer set
F	wait for timer
10	loading to open
11	mecha mode all end

(2) Mecha mode = 2 standby mode

Mecha step	Description
0	stop entry
1	side change check, disc status clear
2	wait for tilt up
3	spindle check
4	wait for slider movement
5	switching the clamp to A-side
6	wait for loading motor operation finish
7	tilt down setting
8	wait for loading motor operation finish
9	move slider to home position
A	spindle check
B	wait for slider movement
C	set loading mode to standby or vertical movement
D	wait for loading motor operation finish
E	mecha mode all end

(3) Mecha mode = 3 stop mode

Mecha step	Description
0	stop entry
1	side change check, disc status clear
2	wait for tilt up
3	spindle check
4	wait for slider movement
5	switching the clamp to A-side
6	wait for loading motor operation finish
7	tilt down setting
8	wait for loading motor operation finish
9	move slider to home position
A	spindle check
B	wait for slider movement
C	power off check
D	wait for loading motor clamp finish
E	mecha mode all end

(4) Mecha mode = 4 disc sense mode

Mecha Step	Description
0	if B-side, to step F if CD or CDV, to step 4
1	LD EQ setting, CAV setting, slider target setting
2	wait for slider movement (LD sense position)
3	wait for focus lock, when locked, confirm LD and go to mecha mode all end
4	wait for focus OFF
5	LD fix or if B-side go to step B, CD EQ setting, slider target setting
6	wait for slider movement (CD sense position)
7	wait for focus lock, when locked, confirm CD and go to mecha mode all end
8	wait for focus OFF
9	LD EQ setting, CAV setting, slider target setting
A	wait for slider movement (LD sense position)
B	if there is no CD direct, go to step E
C	wait for focus lock, when locked, confirm LD and go to mecha mode all end
D	wait for focus OFF
E	set to no disc and go to mecha mode all end
F	slider target setting, if single is confirmed, go to step 13
10	wait for slider movement (B side inside position)
11	wait for focus lock, when locked, confirm LD and go to mecha mode all end
12	wait for focus OFF
13	set to no disc and go to mecha mode all end

(5) Mecha mode = 5 set up mode

Mecha Step	Description
0	slider target setting
1	wait for slider movement (TOC position)
2	spindle start
3	wait for spindle lock, check for LD misclamp also carried out
4	with LD if in read in, read out area, go to step 5 anything else go to step 6
5	after moving slider to program area, go to step 4
6	play mode entry

(6) Mecha mode = 6 TOC read mode

Mecha Step	Description
0	TOC entry
1	read in search (slider REV sending)
2	program area search (16-track forward jump)
3	read in search (4-track REV jump)
4	wait for program area with play, 100ms timer set
5	reading 1st time TNO address
6	wait for spindle lock
7	jump back to lead-in
8	if TOC cannot be read, treat as LD without TOC and go to mecha mode all end
9	1st time initialize to 0 15 second timer setting
A	wait for TOC reading with read in if readable, end if program area, go to next
B	if subcode is readable, 32-track REV jump
C	if subcode is readable, 32-track REV jump
D	if subcode is readable, 32-track REV jump
E	if subcode is readable, 32-track REV jump
F	return to step A
10	set PRD flag, start movement to program area
11	movement play to program area, 15 second timer setting
12	REV × 8 jump from TNO = 0 to IX = 0 generate code error and end

(7) Mecha mode = 7 play mode

Mecha Step	Description
0	play mode entry

(8) Mecha mode = 8 search mode

Mecha Step	Description
0	search mode entry
1	area change (A/V change)
2	area change wait timer setting
3	wait for area change
4	TOC check & TOC data setting
5	track count search entry
6	wait for track count search
7	wait for Tracking Open
8	zig-zag search (high speed)
9	zig-zag search (low speed)
A	wait for Tracking Close
B	send 256 Track SLDR (search outside CD TOC buffers)
C	wait for end of 256 Track SLDR send
D	wait for Tracking Open
E	32-track continuous jumping
F	wait for end of 32-track continuous jumping
10	16-track continuous jumping
11	wait for end of 16-track continuous jumping
12	1-track continuous jumping
13	wait for end of 1-track continuous jumping
14	32-track jumping
15	16-track jumping
16	4-track jumping
17	jump until right before target
18	play until target
19	search error processing
1A	restart at time of target change during search

(9) Mecha mode = E power off mode

Mecha Step	Description
0	stop entry
1	side change check, disc status clear
2	wait for tilt up
3	spindle check
4	wait for slider movement
5	switching the clamp to A-side
6	wait for loading motor operation end
7	tilt down setting
8	wait for loading motor operation end
9	move slider to home position
A	spindle check
B	wait for slider movement
C	power off check
D	wait for loading motor clamp end
E	mecha mode all end

(10) Mecha mode = F recover mode

Mecha Step	Description
0	recover entry
1	spindle hold
2	wait for spindle lock
3	spindle stop
4	spindle stop
5	wait for spindle lock end
6	turn slider movement direction
7	timer setting
8	wait for timer & focus lock check
9	wait for timer & slider movement
A	wait for spindle lock
B	recover error
C	CD/CDV recover mode
D	wait for spindle lock
E	recover error

2.9 OUTLINE OF MODE CONTROL SYSTEM

(1) Mode Control Microcomputer

The processes carried out by the mode control microcomputer (hereafter: mode con; refer to table 9) are shown below.

- ① Main body key/remote control signal process
Main body switching and remote control signals are taken in. Processing is carried out according to the designated key.
- ② FL display
Display of FL tube (refer to table 9) is carried out.
- ③ Screen display
The character generator IC (PD0154A) is controlled and characters are superimposed on screen.
- ④ Control of mechanism control microcomputer
When operation is indicated to mechanism control microcomputer (hereafter: mecha con; refer to table 9), at the same time, time data, level data, and other data are read.
- ⑤ Managing system reset
If there is an abnormality in mecha con communication, system reset is turned on and initial state is returned to.

(2) Theater Mode

This mode is to maintain proper mood when playing LD movie software. By turning the theater switch ON during OPEN/STOP or during play, the following operations are carried out.

- ① The theater LED is lit and the theater mode is entered.
- ② At the same time, the FL OFF LED is lit, and the FL display goes off.
- ③ Two seconds after the key is pressed, the screen display goes off. However, this does not include input displays (program, search, etc.)
- ④ One shot memory at time of turning is not carried out.
- ⑤ At time of play start or turning, TOC is not read.

Due to these operations, the reverse time is shortened and there is less fumbling when movie software, etc. is turned over. Also, since the time from stop to start of play can be reduced, it is effective as a quick start mode for LDs. Further, since this mode functions only for LDs, if a CD is played it will automatically go off.

(3) V-DNR (picture quality adjustment)

Mode con (refer to table 9) transmits NR control steps to mecha con (refer to table 9).

A variable amount is appropriated to video signal Y and C signal in a total of ten steps (0 to 9). The mecha con looks at these steps and sets that actual NR amount.

The relationship between steps and NR values is shown below:

Step	Y - NR	C - NR
0	off	off
1	smallest value	smallest value
⋮	⋮	⋮
5	standard value	standard value
⋮	⋮	⋮
9	largest value	largest value

Table 8: Relationship Between Steps and NR Values

If the mode con is in OFF mode, step 0 is sent to both Y and C. If it is in STANDARD MODE, step 5 is sent to both Y and C. If it is in VARIABLE mode, variability from 0 to 9 is possible for Y signal by shuttling and C signal by jog dial. The selected step is transmitted.

Model	Mode control microcomputer	Mechanism control microcomputer	FL tube
CLD-S360	IC201: PD3248A	IC101: PD0171B	VAW1033
CLD-D503, CLD-D570	IC100: PD3259C	IC101: PD0184B	VAW1032
CLD-D703, CLD-D770	IC100: PD3260C	IC101: PD0185B	VAW1032

Table 9: FL Tube, Mechanism/Mode Control IC Table

3. SERVOS FOR FOCS, TRKG, SLDR

3.1 FOCS SERVO SYSTEM

The focus servo's operation initiation command is sent to the DSP IC (LC78681E) by serial data from the mecha control IC. When the DSP IC receives the command, first the FTS section C987 charge is discharged by FST signal and the object lens is lowered. Next, by a FOCS signal, it is recharged and is gradually pulled up. When focus is achieved, *FZD goes down. When this signal is received, the FOCS signal is reset and the focus servo goes on. (refer to Fig. 3-1-3 and Fig. 3-1-4) (The focus loop SW is in the PAC 003A EQ section.) The operation initiation is the same as

before, but as a condition, FSUM is not used. Even the XFOX signal that goes to the mecha control IC establishes a time constant for the signal created by the FSUM in the PAC 002A interior and outputs it.

There is no large difference with the former FOCS servo system, but the EQ composition has changed and the FOCS does not carry out loop switching in response to DEFECT. refer to Fig. 3-1-1 and 3-1-2 for EQ section (only TRKG system) and SW logic.

FOCS SUM is composed by the AMP in the PAC002A interior and due to the addition of the AGC circuit, the former SUM LEVEL adjustment VR has been eliminated.

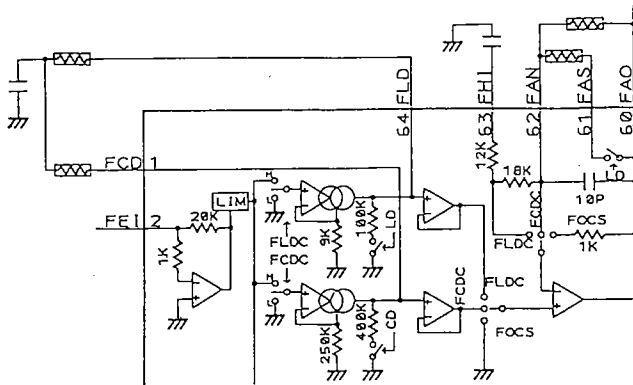


Fig. 3-1-1 FEQ. (FOCS EQUALIZER) Section Circuit

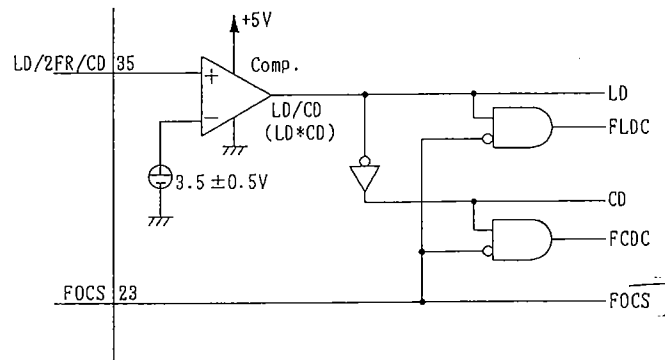


Fig. 3-1-2 FEQ. (FOCS EQUALIZER) Control Logic Circuit Diagram

Disc present

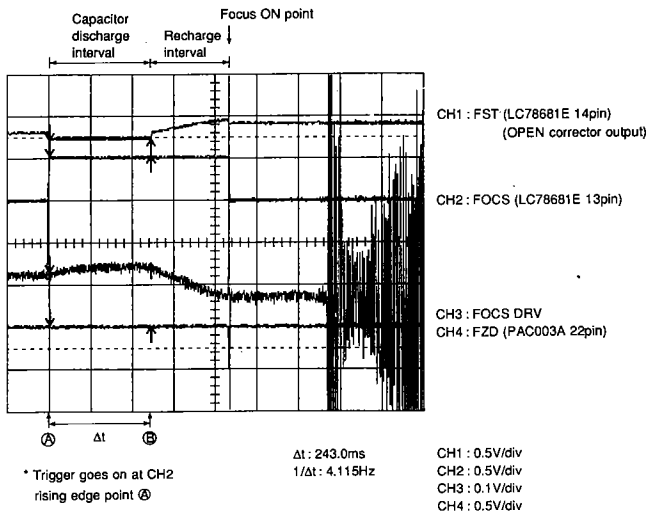


Fig. 3-1-3 FOCS Timing Chart When Disc is Present

No disc

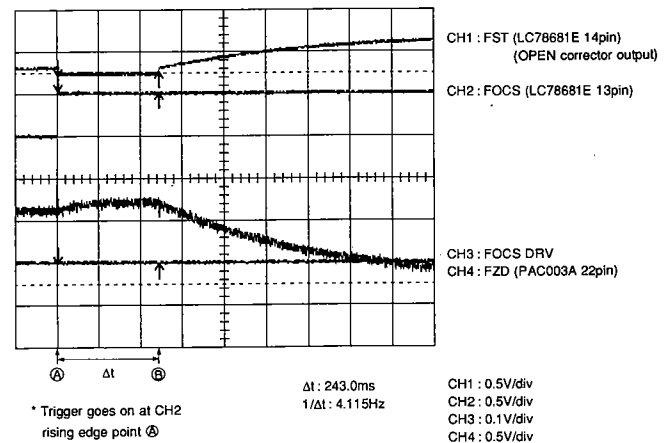


Fig. 3-1-4 FOCS Timing Chart When No Disc is Present

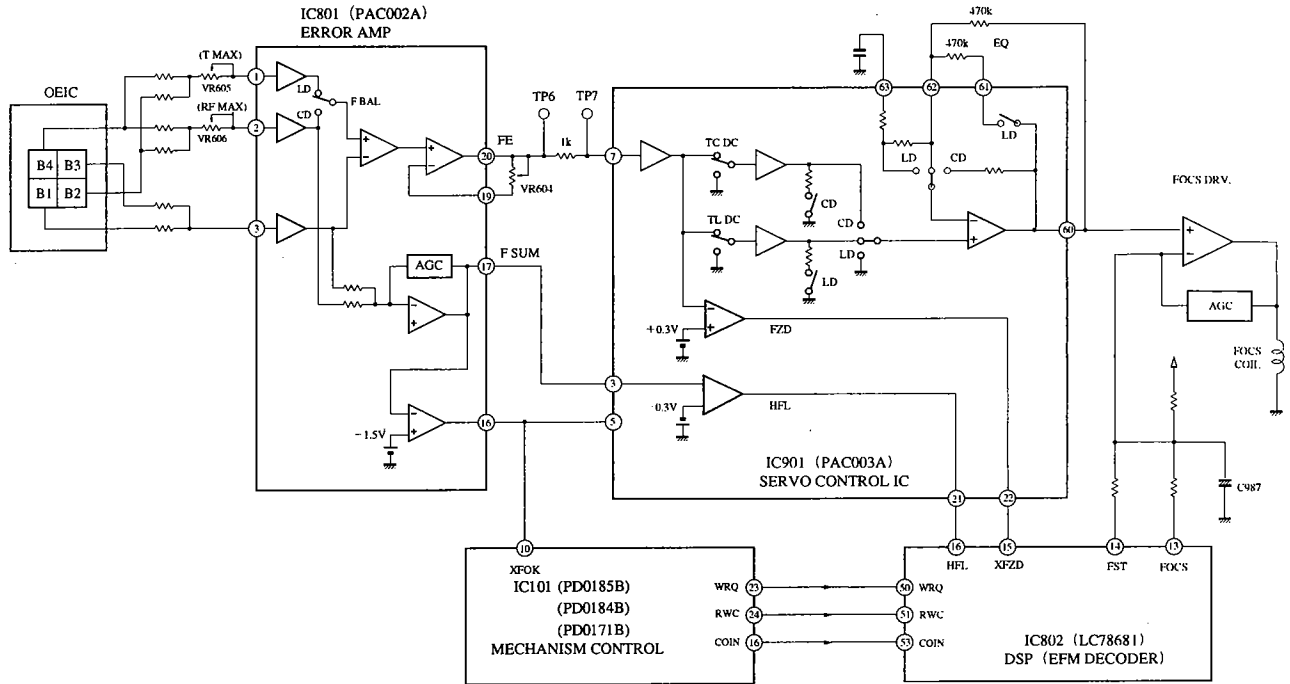


Fig. 3-1-5. FOCS SERVO BLOCK DIAGRAM

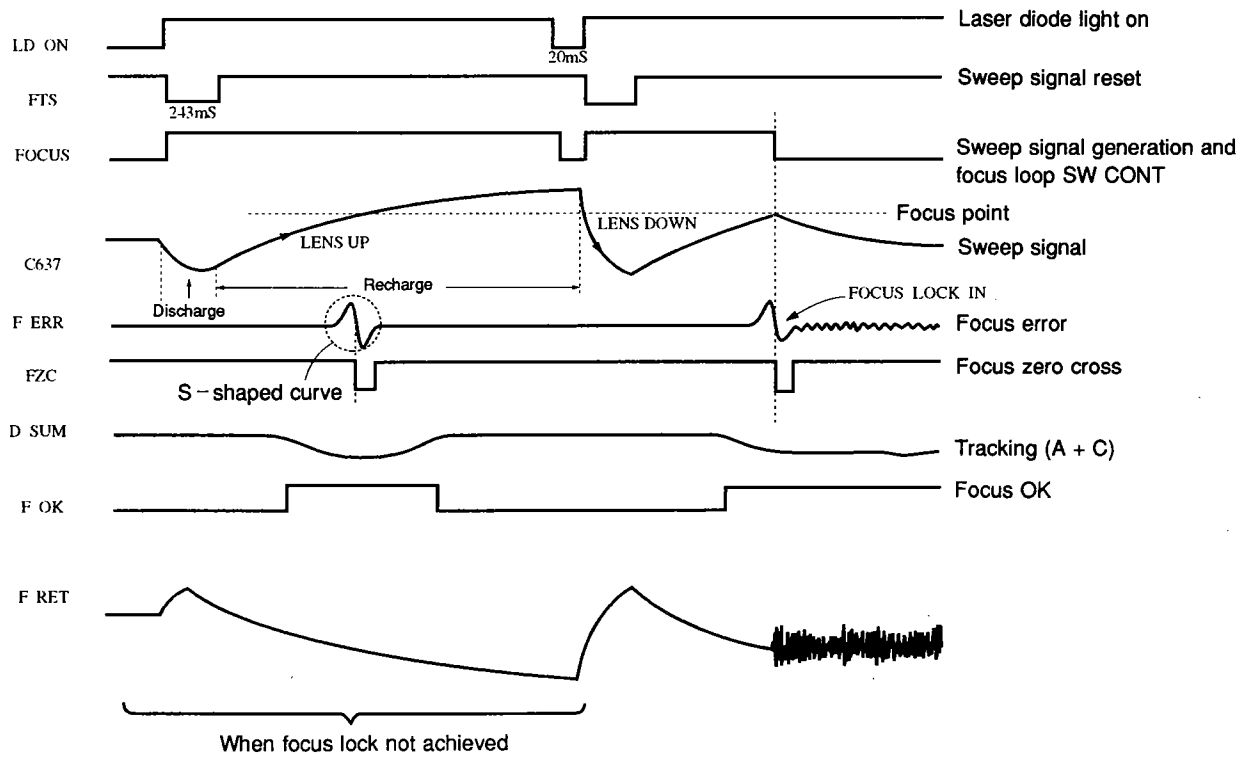


Fig. 3-1-6. FOCS SERVO TIMING CHART

3.2 TRKG SERVO DESCRIPTION

●Signal Flow

A and C output from the OEIC of the PICKUP ASSY is input into 23pin and 24pin of PAC002A and passes through the built-in TRKG error amp and is output through 22pin. PAC002A ATB (AUTO TRKG BALANCE) circuit detection and TRKG offset detection are also carried out. The TRKG error signal that is output from 22pin is input to 7pin of PAC 003A after being gain adjusted by VR603. It then goes through the EQ section and is output from 16pin. In the EQ section, for optimal trackability, interior SW are switched by the logic section signal that is composed of LD/CD, THLD, TGL, TOFF, and DEF signals. The EQ section and logic circuit are shown in Fig. 3-3 and 3-4.

●One Track Jump and Multi-Track Jump

The timing chart for each pin output signal of IC 901 (PAC 003A) at time of One track jump and multi-track jump is shown. (Fig. 3-2) One track jump is the same as in the former model (used PA3003), but in the case of multi-track jump, the timing for turning TRKG servo ON is not by frequency detection. Instead it is by track count detection. In other words, for 32-track jump, the old model would output 16-track portion axle and after that it would be indefinite. In this model, however, even the brake outputs 16-track portion.

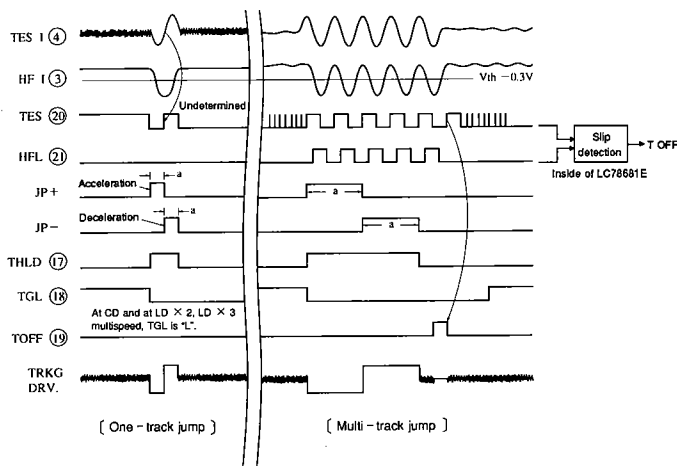


Fig. 3-2 Timing Chart for Each Pin Output Signal

3.3 SLIDER MOTOR CONTROL

●Signal Flow

The tracking drive signal that is output through 1pin of drive IC902 (TA8464K) passes through LPF, is amplified by IC903 (BA4560F). After it is subject to a level shift by the 2.5V center, it is input to IC101 (mecha control IC) 6pin and makes SLDR ERR signal. The slider motor drive pulse that responds to that signal's level is output from 18pin and after being power amplified by drive IC803 (LA6510L), it drives the slider motor.

When the pick up position is forcibly moved at time of disc determination/start, in response to slider position signal that is input to 7pin of IC101, operation is carried out while position is being detected.

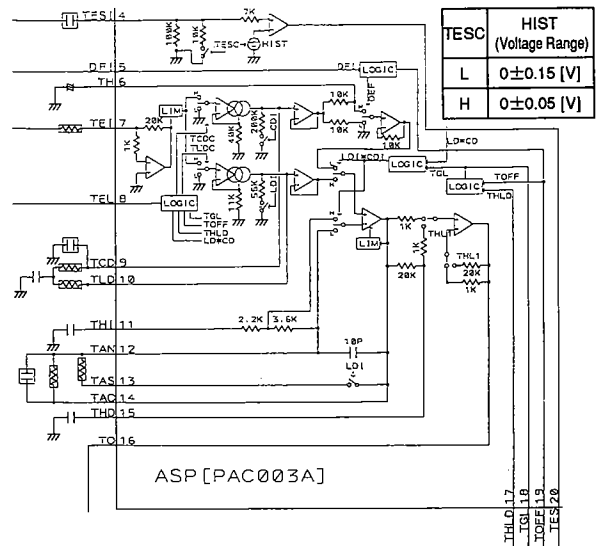


Fig. 3-3 TRKG EQ Section Circuit Diagram

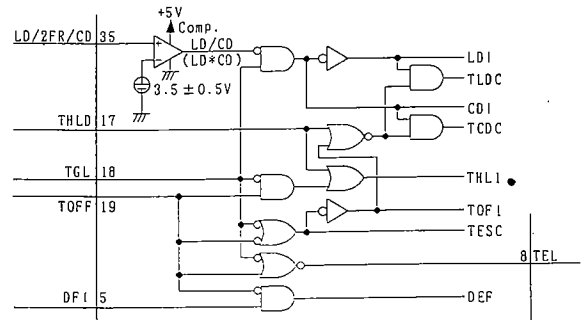


Fig. 3-4 TRKG EQ Control Logic Circuit Diagram

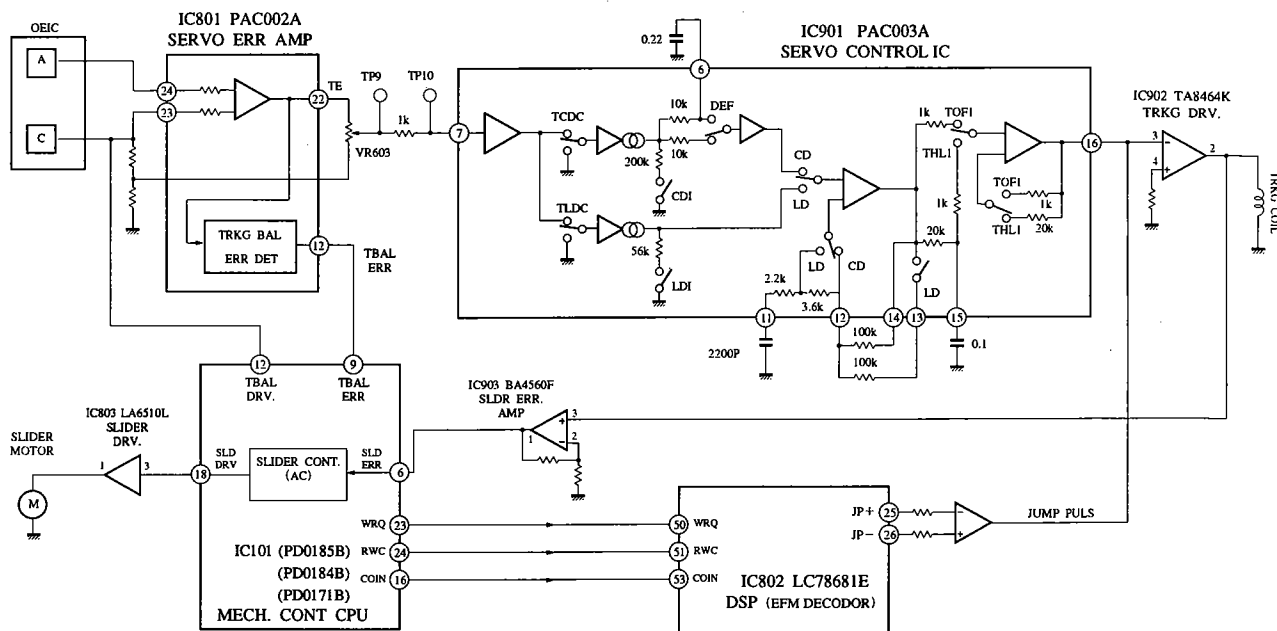


Fig. 3-5 TRKG and SLDR SERVO BLOCK DIAGRAM

4. VIDEO SIGNAL PROCESSING SYSTEM DESCRIPTION

· An explanation of the video signal processing system will follow the block diagram (Fig. 5-1 and 5-2).

4.1 RF SYSTEM

The RF signal from pick up is amplified by the RF - AMP after being RF - Level adjusted. It then undergoes RF correction processing and the main line passes through the audio carrier trap and B.P.F. and is input to PA0023AD. RF for drop out passes through H.P.F. and is input to PA0058A.

4.2 MAIN VIDEO SYSTEM

The video signal that is detected by PA0023AD first goes through L.P.F. and is amplified by approximately 8dB revolving AMP. After passing A/D video level adjustment VR, it is input to PA0058A ②pin.

The video signal input from ②pin is first NR processed and is output from ⑭pin. It then passes A/D PRE - LPF and again is input to PA0058A and is amplified by sync chip clamp and 6dB AMP. From there it is output from ⑫pin and is input to PD 0146A.

4.3 DROP OUT SYSTEM

The DOS RF signal that is input to PA0058A ②pin undergoes level and frequency sensing. Drop out pulse is output from ② pin and in PD0146A, drop out compensation is carried out. Also, at the same time as ②pin output, CLAMP pulse in PA 0058A is suppressed.

4.4 SYNC SEP AND DATA SEP SYSTEM

The video signal that is NR processed in PA0058A passes through L.P.F. and is output from ⑧pin. Due to SYNC SEP and DATA SEP, it is again input from ⑤ and ⑥pin. With the video signal that is input from ⑤pin, CLAMP PULSE is made. With this pulse, pedestal clamping is done for the video signal that is input from ⑥pin. From this signal, SYNC and DATA are extracted. The output SYNC is composite SYNC and is input to PD0146A of next step and is synchronously separated into V and H.

5. TBC SYSTEM DESCRIPTION

5.1 DIGITAL VIDEO PROCESSOR (DVP : PD0146A)

With CLD - D703, CLD - D503, CLD - D770, CLD - D570 AND CLD - S360, time axis correction (spindle error generation, TBC) and picture signal processing are carried out in PD0146A. This IC's main functions are as follows.

- Generation of axle control signal
- Generation of spindle error
- Horizontal and vertical sync separation
- Spindle driver I/F
- Digital TBC
- Color drop out compensation
- SSG (sync signal generator; sync generation)
- Background color generation and squelch switching
- Character insertion
- Error generation for ACOM (audio compensation)

However, between the model with the video memory system (CLD - D703) and models with only base systems (CLD - S360, CLD - D503), there are differences in some of the functions. In the model with the video memory system, character insertion, 140ns shift, etc. signal processing is carried out in PD3212A. (refer to Fig. 5-1 and 5-2).

5.2 SPINDLE CONTROL

· Axle Control Signal Generation

In response to forced acceleration/deceleration signal from the mecha control IC, video FM carrier frequency detection result during RF signal, and cycle detection result of the PBH that was separated from PBC SYNC, axle control signals are generated. The threshold value of RF frequency detection is attached with hysteresis and at NG → OK it is [7.57MHz, 9.34MHz] and at OK → NG it is [6.43MHz, 10.72MHz]. The PBH cycle threshold value is similar; at cycle detection NG → OK, it is [62.4μs, 64.9μs], and at OK → NG, it is [60.5μs, 65.9μs].

Also, this signal's duty control can be carried out by serial command from the mecha control IC.

· Spindle Error Generation

The parity pulse from PBC SYNC is masked and is compared with sync separated PBH and REF H and frequency/phase error for three state outputs is generated. However, when motor drive is suppressed, at RF frequency NG, and during jump operation, a duty 50% signal is output. The phase comparison range is 120μSp-p or more.

· Gain Control Signal Generation

A signal for gain control of spindle servo loop is output through control of mecha control IC.

· H,V Sync Separation

From PBC SYNC that is input from PA0058A, H sync and V sync are separated. H sync is masked with parity pulse and separated. That mask amplitude is 58.3μs when RF frequency detection and H sync cycle detection is OK, and 48.7μs when NG. Further, V sync detection delay time is $0.5H < T < 1H$.

· Spindle Driver I/F

The spindle error PWM conversion signal PWMI that is output from PAC003A and the forward/reverse signal F/R are converted to signal for spindle driver use and then output through DRVA and DRVB.

For the prevention of a current going through the driver, a delay time for ON can be set by the mecha control IC.

5.3 DIGITAL TBC

A big difference in this PD0146A digital TBC system and the former digital TBC system is the fact that the PLL for clock generation for writing to FIFO has been largely digitized. The fsc that followed the jitter of the video signal on the side that was written by PLL from the digital video data that was sampled by the A/D converter is generated. It is then successively multiplied 4 times and becomes sampling clock of A/D converter and writing clock of FIFO. Also, the digital video data that is written into FIFO with this clock is read by the standard 4fsc clock. Then, play back and color back switching, 140ns shift, character insertion, etc. are carried out and output is done through both 8bit digital output and analog output. However, since sync cannot be inserted into the output video signal, sync insertion must be done outside.

Also, for writing clock generation, in addition to feed back (digital PLL), there is also feed forward method (DPS; digital phase shift). Determination of TBC LOCK can be done through spindle system RF frequency detection result, H sync period detection result, and PLL for TOC. In each case, at time of OK condition, "Hi" is output.

5.4 SSG

Insertion composite sync (open drain output) and delay amount variability composite sync are output. Through mecha control IC, with base system, SSG responds to trick play by manipulation of reset shift, etc. With a memory system, SSG is at free run and it is possible to carry out field change by FCH input from PD3124.

VIDEO & TBC BLOCK DIAGRAM

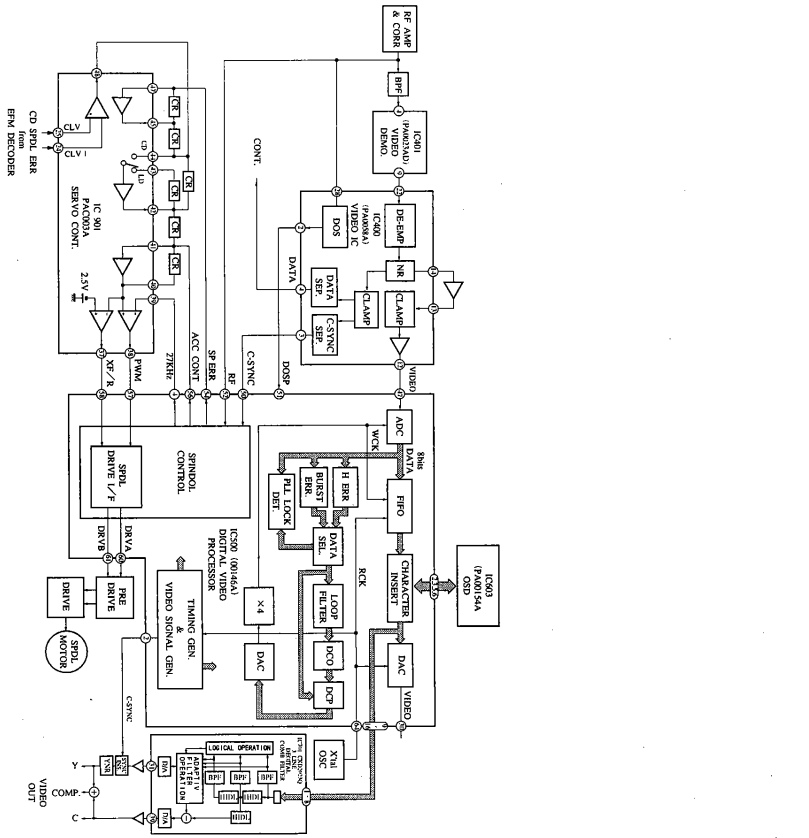


Fig. 5-1 CLD-D503, CLD-D570 AND CLD-S360 VIDEO AND TBC BLOCK DIAGRAM

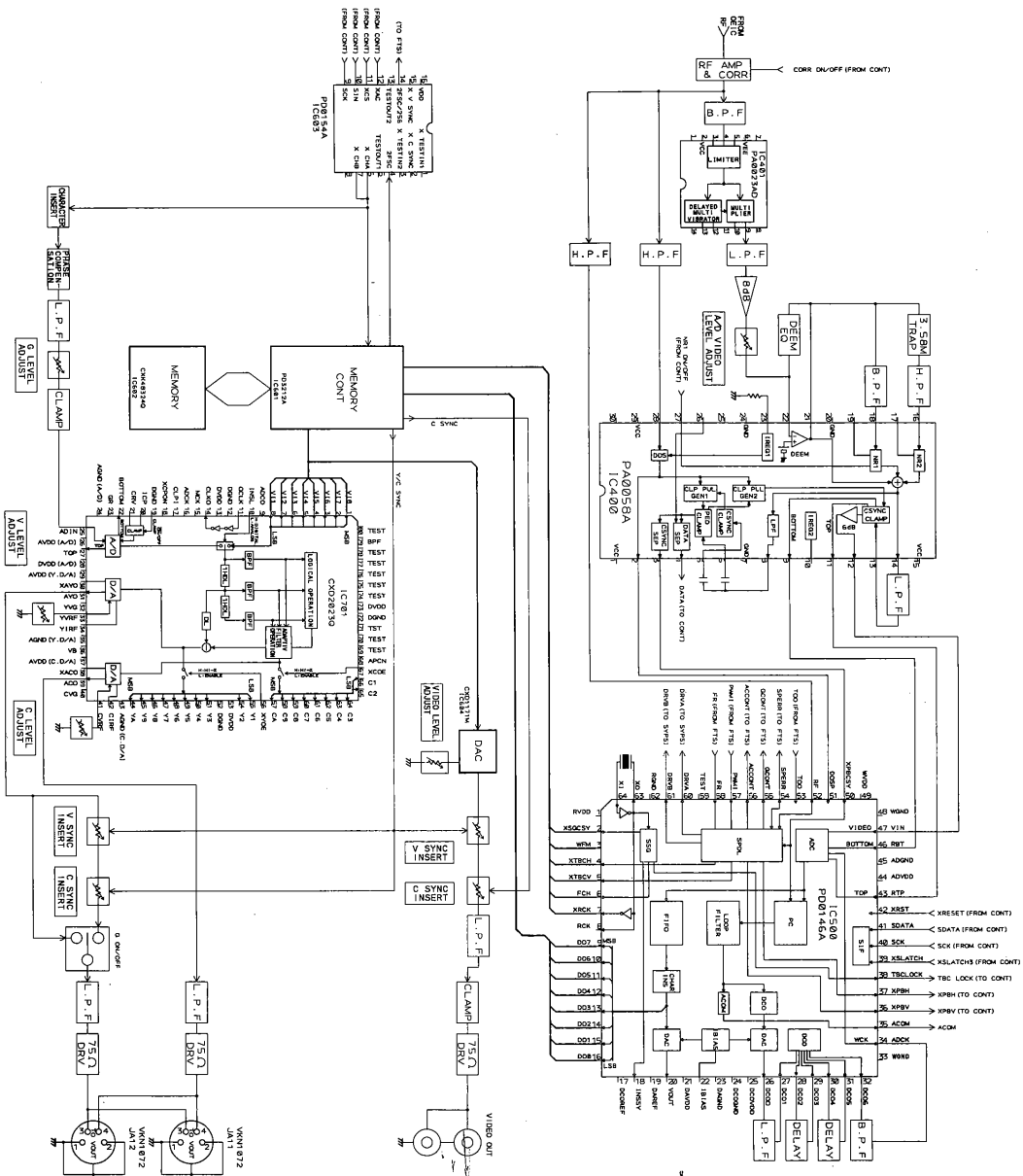


Fig. 5-2 CLD-D703 AND CLD-D770 VIDEO AND TBC BLOCK DIAGRAM

CLD-D703, CLD-D503, CLD-D770, CLD-D570, CLD-S360

VIDEO MEMORY SYSTEM DESCRIPTION

CLD - D703 and CLD - D770 only)

MEMORY CONTROL IC (PD3212A)

The digital 8bit video signal that is time axis compensated, synchronizes processing and field circuit noise reduction processing are carried out simultaneously by the memory control IC (PD3212A) and the 3 - PORT 2M bit video RAM (48334Q). (refer to Fig. 6 - 1)

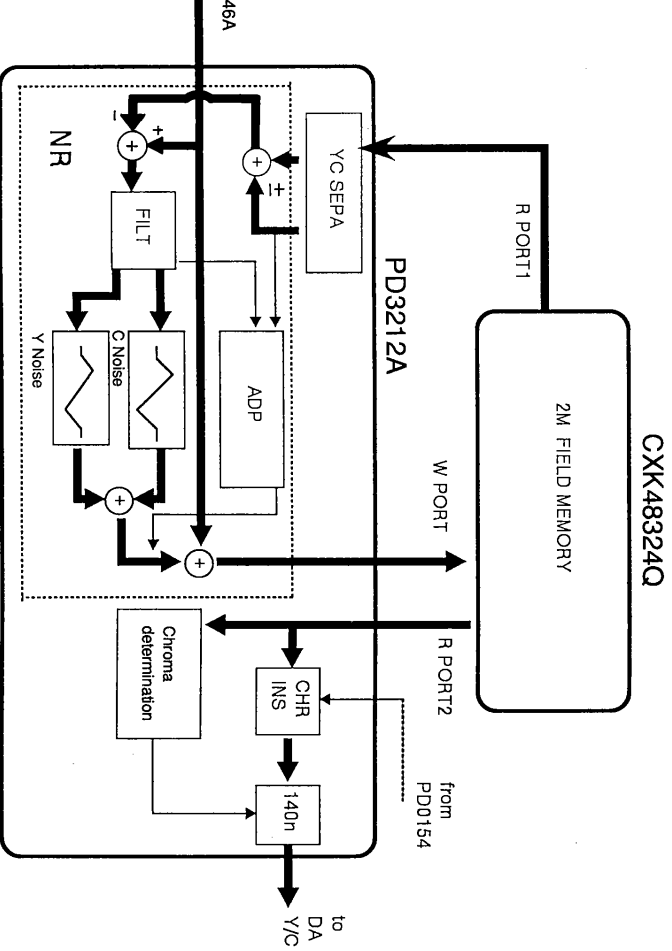


Fig. 6 - 1. Memory Control Section Block Diagram (CLD - D703 and CLD - D770 only)

6.2 FIELD CIRCUIT DIGITAL NOISE REDUCTION

Although the noise reduction function is similar to that of the formerly used PDB033A, the Y/C separator for chroma reverse function that is necessary for NR is built into PD3212A.

1) Signal Flow

The 8bit digital video data taken from the DVP (digital video processor) is subtracted from the data of 1 field back that was read from the R port of memory. Difference datum is created. After the difference datum is separated into C noise and Y noise by the digital filter, each enter a non-linear circuit and compensation data for NR use are created. After these two video data that was process time delayed and the noise component is negated.

2) Y/C Separator for Chroma Reverse Use

In NR, difference datum must be obtained by subtracting from the datum of one field back, but for this, the chroma phase of subtracted data must match each other.

With NTSC video signal, for each 1H, the chroma phase is revolved 180 degrees and because field memory is taken in 263H and 262H increments, the data before subtraction comes alternately as same phase/opposite phase.

To match these phases, the data from one field back that is read from memory is run through the Y/C separator and separated into Y and C. Then, C revolves or does not revolve depending on the field and after being added to Y, it is subtracted from the present video. refer to Fig. 6 - 2.

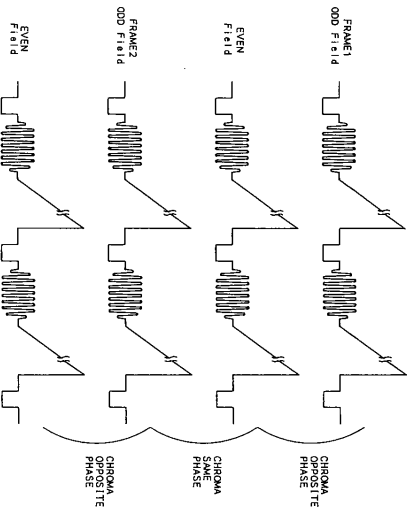


Fig. 6 - 2

3) Adaptive Processing

With field or frame circuit NR, the moving pictures' correlativity is lowered, and there is blurriness and other picture distortion. To prevent this, at time of adaptive ON (serial control ADP ON), the picture color level and movement is detected and NR for each picture element is turned ON or OFF. That detection level is set by serial command ADCL 0 - 2 and ADYL 0 - 3.

4) Non-Linear Circuit Limiter Level

The limiter level for non-linear circuit of C noise and Y noise is each set by serial command CL 0 - 4 and YL 0 - 3.

6.3 FIELD SYNCHRONIZE PROCESSING

The video data that is input from the DVP goes through the NR section, and TBCH and TBCV are synchronized and written to field memory. For reading, it is synchronized with SG SYNC and read out through R port 2. Through control of writing timing, even at time of trick playing, the picture can be output with not great distortion.

1) Field Manipulation

Memory is in field units and the polarity of the read out field is not necessarily the same as the field polarity of SG SYNC. (i.e., for ODD sync, EVEN video data is read out)
 In such case, the read data is delayed 1H on one side to prevent distortion on the screen.
 Also, in that case, at PLAY, FCH signal is sent to DVP and SG SYNC polarity is changed.

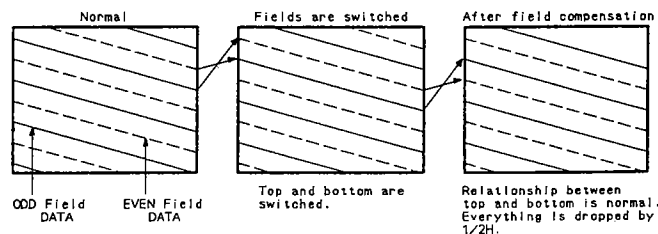


Fig. 6-3

2) Field Compensation Segment

In the case when one side field screen is interlaced and output, as in CLV still pictures, in order to improve bad vertical resolution, the middle value of 2H forward and back is sent out. It is controlled by the serial command INTP.

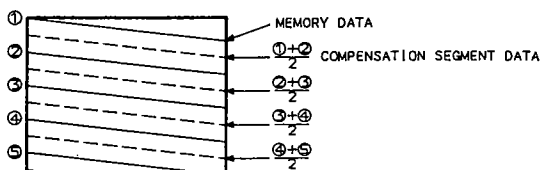


Fig. 6-4

3) Character Insert

A character timing signal (CHA, CHB) is received from the OSD (on-screen display) IC PD0154A and the prescribed video level is switched to and characters or background can be inserted.

4) Determination of Reading Chroma/140ns Shift

The continuity of the burst of the video signal read from port 2 is determined. Normally, three peak points of the burst and 3H from peak is determined. In the case when polarity of all these values are different in relationship to previous values, the determination signal is revolved and the data and the 140nsec shift of the insertion sync are turned ON/OFF. Consequently, this goes into operation at time of trick play and video data with continuous chroma is automatically output.

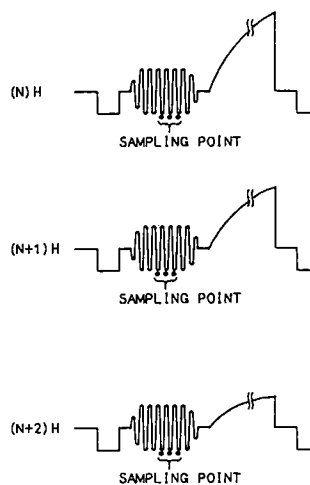
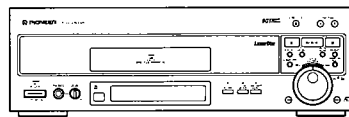


Fig. 6-5

5) Sync Delay

If 3-line Y/C separator is in effect in second step, since data is delayed 1H, insert SYNC (YC SYNC) output is also delayed by 1H and YC to match.

Service Manual



SERVICE GUIDE

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CLD-D770

CLD-D570

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1. OVERALL BLOCK DIAGRAM

1.1 OVERALL BLOCK DIAGRAM FOR CLD-D503, CLD-D570 AND CLD-S360

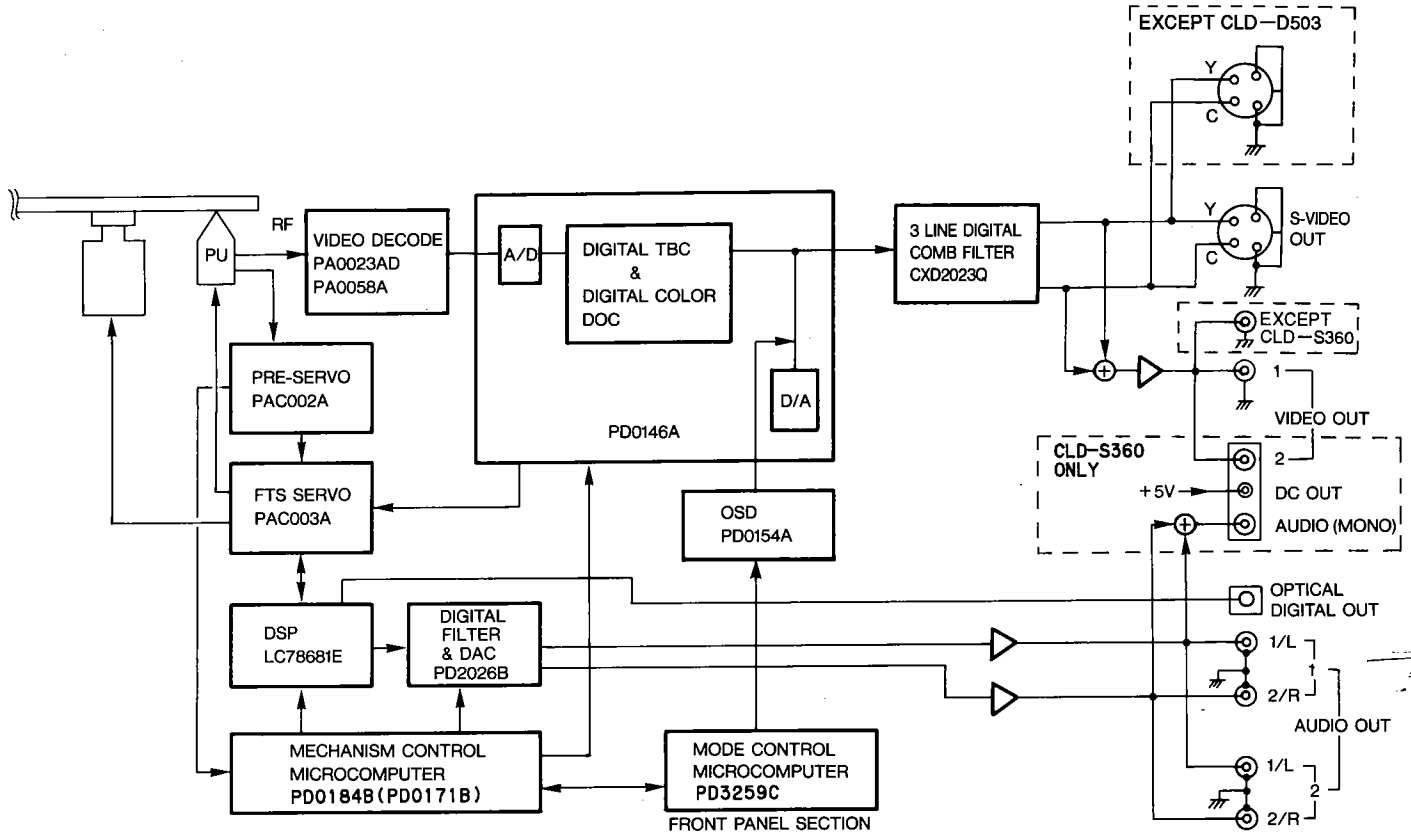


Fig. 1-1 OVERALL BLOCK DIAGRAM FOR CLD-D503, CLD-D570 AND CLD-S360