A NEW DIGITAL VIDEO SIGNAL PROCESSING SYSTEM FOR A VIDEO DISC PLAYER

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ABSTRACT

This report describes a video signal processing system for video disc players we developed on the basis of a new feed forward technique.

The new system is composed of two LSI units: a signal processor for the TBC (time base corrector) which constitutes the basic block incorporating A/D and D/A converters; and an LSI including the FNR (field noise reducer), for additional functions using a field memory.

1. INTRODUCTION

Video signal processing is one of the most important functions of a video disc player. A video signal is recorded as a composite signal on a video disc by the direct FM method; therefore, the video signal tends to suffer from color phase irregularity due to the high frequency jitter caused by disc eccentricity . Furthermore, disc noise, if remaining in the video signal, is a problem for TV viewers.

Thus, effective removal of jitter and noise from a video signal has been a big challenge in developing a video signal processing system. The other requirements of a video signal processing system are the reduction in the number of components and high extensibility.

To meet these requirements, we have developed a new video signal processing system . Using feed forward technique and digital technology, the system improves picture quality, and is highly extensible in that the basic block can be further developed to provide additional functions.

The system features are as follows :

1. A basic block that utilizes only an LSI unit for digital TBC containing A/D and D/A converters;
2. A new feed forward time base error corrector adaptable for still pictures and FNR;
3. An FNR that shares memory with a field synchronizer and is capable of processing composite signals; and
4. A linear-phase digital noise canceler with high waveform reproducibility.

2. SYSTEM CONSTRUCTION

Fig. 1 is a block diagram of the entire system we developed. The master clock frequency of the system is 4 times the color sub-carrier frequency (4Fsc = 14.31818 MHz); the video signal is quantized into eight bits. The system can be realized by two LSI units.

2-1 Basic Block

The basic block is realized by an LSI for digital TBC having A/D and D/A converters. An FM signal detected by the pickup is demodulated, and is input to the built-in eight-bit A/D

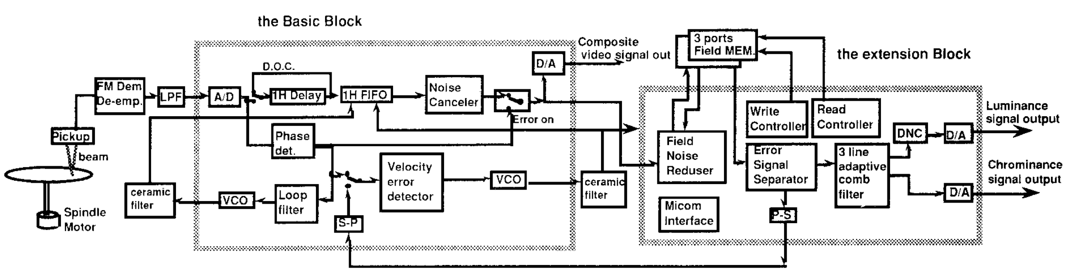

Fig1 The block diagram of the entire system

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converter. After dropout compensation, the input signal is written in the FIFO (first input first output) memory, in response to a clock pulse generated by the built-in digital PLL (phase-locked-loop) circuit. The clock pulse follows the jitter of the input video signal. The PLL circuit comprises phase comparators, a loop filter and a VCO (Voltage Controlled Oscillator). All the components of the PLL are realized by digital circuitry except for the VCO filter.

The phase comparators of the PLL circuit are of two types: a first phase comparator for detecting the time base error using a horizontal synchronization signal, and a second phase comparator for detecting the time base error using a burst signal. For time base error detection, the system uses the burst phase comparator after stable rotation of the motor. The construction of the burst phase comparator is shown in Fig. 2

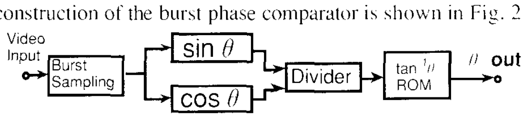


Fig2 Burst phase comparator

This comparator samples a burst signal and a sine and a cosine terms are separated from a burst signal. Based on the result of division between these terms, an arc tangent circuit calculates the phase angle of the time base error. An arc tangent circuit is composed of a ROM(Read Only Memory).[1]

Fig. 3 shows the circuit construction of the digital VCO.

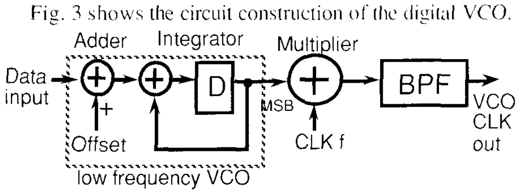


Fig 3 The VCO

The low frequency VCO comprises an adder and an integrator. The multiplier converts the frequency of the output of the low frequency VCO, and the system clock (4 Fsc) is separated from the multiplier output by an analog filter .

However, when an input signal is written in the FIFO memory, the lag time in the feedback system results in insufficient gain of the loop at high frequencies, thus high-frequency jitter cannot be removed.

In the new system we developed, therefore, the reading clock output from the digital VCO for reading is phase-modulated according to the residual jitter (so as to constitute a feed forward system). Thus this method enables the new system to remove the jitter contained in the read video signal at high accuracy.

The system can effectively suppress residual jitter at high frequency by employing the velocity error compensation method as well. In this method, jitter error in a 1H period(1 horizontal scanning period) is obtained through linear interpolation.

Fig. 4 shows the jitter suppression characteristic of the system, with frequency along the X axis and jitter suppression level along the Y axis. (A) is the characteristic with the PLL circuit alone; (B) is the characteristic with the phase-modulated reading clock.

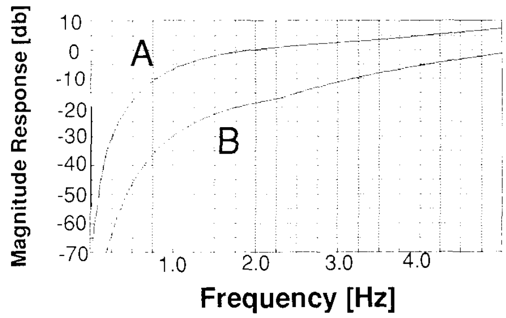


Fig4 the jitter suppression characteristic

In the last stage, the video signal read from the FIFO is input to the noise canceler circuit, which reduces the disc noise and the mixed modulation noise of the FM audio signal in the video signal. The video signal is then output from the built-in eight-bit D/A converter.

2-2 Extension Block

The extension block, which receives the eight-bit digital data output from the basic block, operates in response to a reading clock generated in the basic block. It provides two primary functions: a field synchronizer and an FNR, both of which use a same 2M-bit field memory.

Video signal inputs are sequentially stored in the field memory, and are read from the memory based on the reference signal. Thus, the extension block allows a special reproduction function for still pictures and stable searching of CLV (constant linear velocity) formatted discs.

The extension block uses three-port memory. One of its outputs is fed back to the input side through the extension block, constituting an FNR circuit. An FNR improves the picture quality of video signals passing through the circuit.

The video signal output from the memory is input to a three-line adaptive comb filter. The three line adaptive comb filter separates the input video signal into the Luminance (Y) and chrominance (C) signals. The luminance signal obtained after Y/C separation is passed through a special noise canceler circuit, and is output from a D/A converter for the luminance signal after elimination of minor noise. The chrominance signal is output from a D/A converter for the chrominance signal.

When these signals are output from the respective D/A converters, the clocks of the converters are phase-modulated, in accordance with the residual jitter, by the clock modulation circuit of the basic block. Accordingly, the jitter is removed at high accuracy from the video signal.

3. NEW TECHNOLOGY

3-1 New Feed-Forward Time Base Error Corrector

Conventional feed forward time base error correction has the problem that D/A conversion must be conducted immediately after the detection of time base error.

Specifically, if the field memory is located between the time base error detection circuit and the D/A converter, the video data, having passed through the field memory ,will not correspond to the residual jitter information detected before the field memory. Consequently, the clock for the output video signals will be modulated on the basis of inappropriate data. Thus the jitter remains.

Also, if the field memory is located between these circuits and the D/A converter, a residual jitter detection circuit will be needed immediately before the D/A converter, resulting in duplicate circuitry.

The new system has solved these problems by employing the new time base error correction method described in the following.

According to this method, the time base error information detected in the basic block is superposed on the horizontal synchronization signal of the video signal, as shown in Fig. 5.

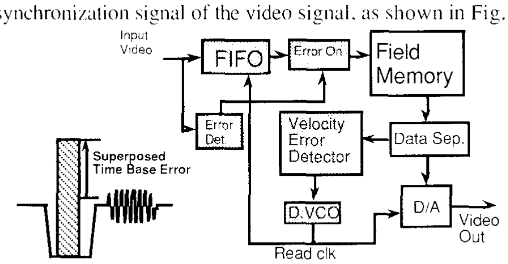


Fig5 Fig6

New feed forward time base error corrector

Here, the data superposed is detected and inserted in the basic block . The level of the superposed error data corresponds to the amount of time base error . The width of the superposition is about 2usec based on the falling edge of the horizontal synchronization signal; this allows stable sampling of the error data from the video signal output from the field memory.

Fig. 6 shows the circuit construction of the new feed forward time base error corrector.

After the video data is read from the memory, the superposed data is taken and is fed back in the form of serial data to the basic block. On the basis of the data thus fed back, linear interpolation is conducted for a 1H period to calculate the velocity error. The clock generation circuit of the basic block phase-modulates the clock according to the calculated velocity error. The horizontal synchronization signal component of the video signal is then returned to the original state after the data is taken.

This technique permits proper velocity error correction, even with a synchronizer that continuously outputs video signals from the field memory.

Furthermore, the system with the circuit construction described above can process not only video signals but also error information for field noise reduction (as described below). Consequently, the processed error information corresponds to the processed video signal, thus permitting both field noise reduction and feed forward time base error correction.

In short, the new system does not restrict circuit construction, nor does it require any additional circuits before the D/A circuit, and it is compatible with various operation functions.

3-2 Field Noise Reducer

The new system consists of a feedback field noise reducer (FNR), using the field memory of the synchronizer.

This FNR is characterized in that:

(1) it is capable of processing composite signals,
(2) it is adaptable to the feed forward time base error correction method ,
(3) it shares memory with the synchronizer,and,
(4) it can operate even in special reproduction by frame.

Due to these characteristics, the FNR provides efficient circuit construction, permitting substantial noise reduction in the video signals of video discs.

Fig. 7 shows the circuit construction of the FNR.

The FNR comprises ,a field memory, a burst phase detector, a chroma inverter, a filter, coefficient circuits. The circuit uses three-port memory, having 1 input-port and 2 output-ports.One of the two outputs is fed back for field noise reduction.

If a video signal feedback delay set at 262H or set at 263H, some noise would move up or down in the picture. Therefore, the FNR of the new system selects either 262H or 263H for the delay in each field alternately.

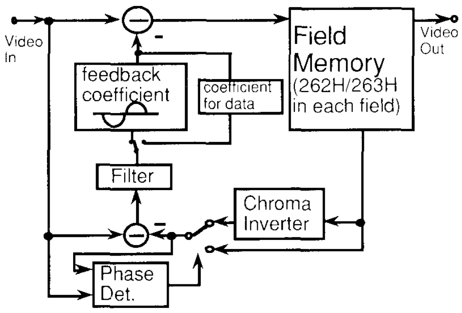


Fig7 The Field Noise Reducer

Then, in order to detect the non-correlative portion, subtraction is conducted between the input video signals and the feedback video signals .

However, it is necessary to adjust the phase of the burst signal before the detection of correlation if the circuit processes composite video signals.

Therefore, the FNR compares the burst phase between the video signal output from the memory and the input video signal before the detection of correlation, and if the burst phases of the signals do not agree, the chroma-inverter circuit is selected.

That is, when the delay in a particular field is 263H, the video signal is passed through the chroma-inverter for the field.

This method works effectively for video disc players with which memory play is common. Specifically, in slow reproduction or jog reproduction by frame, since the burst phase has been detected, the FNR can be operated with no problems despite the discontinuous fields of the reproduced video signals.

The chroma-inverter circuit is a filter for inverting the phase of the carrier chrominance signal range alone.

The transfer function is expressed by the equation:

$$H(z) = \frac{(1+Z^{-4})}{4}$$

This circuit provides the characteristic shown in Fig. 8.

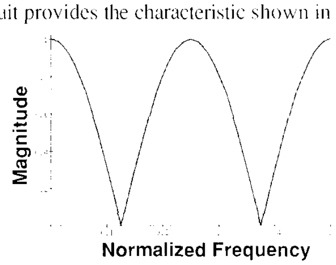


Fig8 The chroma inverter

in which 0.25 corresponds to the color sub-carrier frequency because the axis for frequency is normalized.

However, there are two problems to be solved: the deterioration of vertical resolution and the after image.

The deterioration of the vertical resolution occurs when the detected non-correlative portion contains a vertical signal component as well as noise.

To prevent deterioration of the vertical signal component, a filter is used for the non-correlative signal. This filter, a high-pass filter, lowers the gain for the luminance signal in the low frequency range, preventing the deterioration of vertical resolution.

The signal output from the high-pass filter is input to the feedback coefficient circuit of the FNR. The feedback coefficient is adaptive, changing the gain according to the input level. It is set to provide a smaller output for an input of larger amplitude, thus minimizing the after image. The feedback coefficient is realized by a ROM table. And the output of the coefficient circuit is subtracted from the input video signals.

With the above-mentioned construction, the FNR is capable of processing video signals as composite signals, permitting effective reduction of noise in both luminance and chrominance signals.

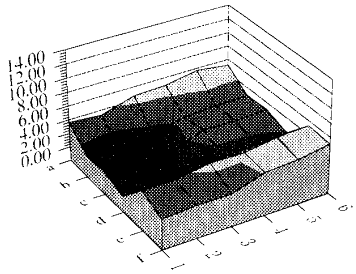
In addition, the FNR can also process the time base error superposed on the video signal. A feedback coefficient circuit different from the one for the video signal is switched for the superposed time base error, as shown in Fig. 7. This is because of the difference in non-correlative information between the video signal and the time base error. The optimum feedback coefficient for the time base error was obtained experimentally.

Due to the feedback coefficient exclusive for the time base error, the feed forward time base correction function works effectively even when the FNR operates, so that the PM noise level is improved.

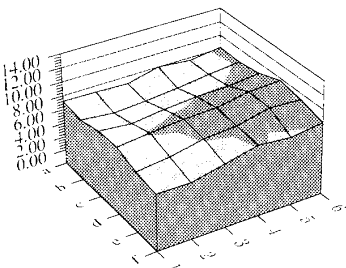
Some examples of improved PM noise are shown in Fig. 9. A TV screen was divided into 25 parts, and the S/N was measured for each part. The measurements are indicated three-dimensionally, with the Z axis representing the improvement in S/N of the chrominance signal, and the X and Y axis corresponding to the horizontal and vertical scanning axis, respectively.

Chart (1) is for a case in which the PLL alone operates chart (2) for FNR alone operates, and chart (3) for both FNR and feed forward time base error corrector operates.

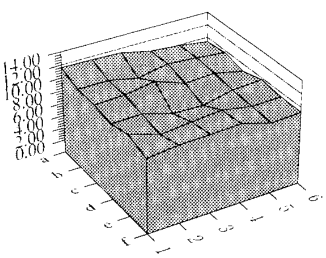
It is clear from these charts that the PM noise level is improved substantially by the FNR, and is improved even more by the feed forward time base error corrector.



(1) PLL



(2) PLL + FNR



(3) PLL + FNR &FF TBC

Fig9 Improvement of PM noise level

3-3 Digital Noise Canceler

In addition to the FNR described above, the new system contains a digital noise canceler circuit to minimize noise in video signals.

Fig. 10 shows the construction of the circuit.

The circuit comprises two different filters, limiters and adders.

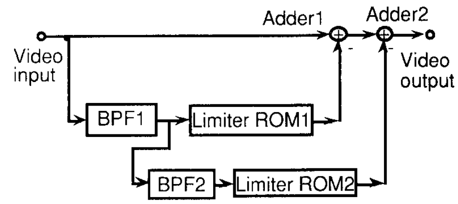


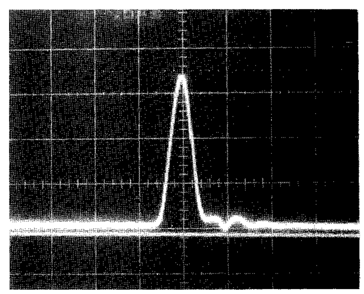
Fig10 The digital noise canceler

In the circuit, the video signal component taken by the filters is input to the limiter , and the output of the limiter is subtracted from the original video signal. The limiter is realized by a ROM.

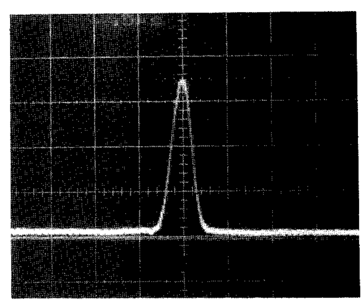
This digital noise canceler circuit reduces not only the disc noise but also the mixed modulation noise of video signal and FM audio signal, in the video signal.

Due to the linear phase, this circuit provides high waveform reproducibility without the ringing and signal distortion which occur in conventional analog circuits, as shown in Fig. 11.

(A) is the waveform through the conventional analog noise canceler, (B) is the waveform through the digital noise canceler.



(A)



(B)

Fig11 the waveform reproducibility

In addition, because of the LSI construction of the circuit, the number of components used outside the LSI has been decreased substantially.

In the extension block, the digital noise canceler circuit for the luminance signal output is provided after the Y/C separation circuit. This construction helps remove the remaining noise of the chrominance signal from the luminance signal, thus improving the S/N of the composite signal obtained by adding the luminance and chrominance signals.

3-4 Three-Line Adaptive Comb Filter

The extension block uses two 1H memories to constitute a three-line adaptive comb filter. This filter, despite its small number of components, is superior in separating luminance and chrominance signals. An selectable band-pass filter for the chrominance signal permits optimum color-bleeding and visibility.

3-5 Built-in A/D and D/A Converters

The new system is of two-chip LSI construction: composed entirely of integrated circuits. It uses C-MOS circuits, with A/D and D/A converters mounted on one chip. The basic block contains A/D and D/A converters, while the extension block contains two D/A converters for luminance and chrominance signals, respectively.

The A/D converter is of the eight-bit type ,with the maximum conversion rate of 20 MSPS, and is low in power dissipation.The D/A converters are of the eight-bit type, with a maximum conversion rate of 35 MSPS.

4. CONCLUSIONS

We have developed and actually realized the video signal processing system described above, which provides the following advantages:

1. One-chip digital TBC
   A one-chip digital TBC LSI containing A/D and D/A converters has been realized for the first time in the world.
2. Feed forward time base error correction is adaptable for an FNR operation
   The system permits feed forward time base error correction adaptable for an FNR operation, thus achieving substantial improvement in the PM noise level of chrominance signals.
3. Improved S/N of luminance and chrominance signals.
   The FNR improves the S/N of luminance signals and the AM noise level and PM noise level of chrominance signals.
4. Adjustment-free system
   Since the entire system is digitalized, it always provides stable performance under various environmental conditions, with no need for adjustment.
5. Reduction in the number of components
   Because of the LSI construction of the processing circuits, the system has fewer components.

Thus, using digital technology, we have realized a highly extensible, high-performance video signal processing system that substantially improves the picture quality of video disc players.

5. ACKNOWLEDGEMENT

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6. REFERENCE

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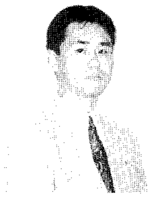
7. BIOGRAPHY

Nobuyuki Ogawa was born in 1958, in Chiba Japan. He received his B.E. degree in electric engineering from Keio university Tokyo Japan in 1980.

In April 1980, he joined Matsushita Electric Industrial Co.,Ltd. He has been developing Video Disc Players at Disc division.



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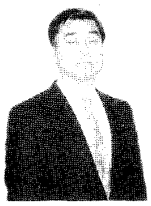

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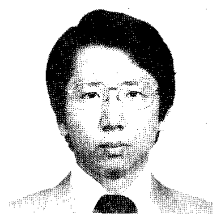

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