CCD DELAY LINE FOR VIDEO TBC

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1. Introduction

Up to now, TBC (Time Base Corrector) of optical video disc player has been made of mirror and coil. This mechanical TBC has disadvantages of high power dissipation, and delicateness against shock or vibration. Since a reliable TBC has been demanded, we have developed an electronic variable delay line using CCD in order to replace the mechanical TBC.

2. Device characteristics

2-1. Physical characteristics and operating conditions

The physical characteristics and operating conditions of the signal processor are shown in Table 1. This IC is manufactured by CMOS-CCD process. The chip size is 3.92 mm X 2.84 mm. The package is 24 pin DIP. Power supplies are 5 V and 9 V. The allowable deviation of both power supplies are less than 5 % of each voltage. The clock frequency range is from 15.2 MHz to 27.2 MHz. The delay time of this IC is variable from 50.1 μsec to 89.7 μsec by changing the clock frequency. Consequently, this IC can correct the jitters of about ± 20 μsec. The maximum allowable input amplitude is 1.28 Vp-p.

Structure	CMOS-CCD
Chip size	3.92mm X 2.84mm
Package	24 Pin DIP
Power supply voltage	9 V ± 5% 5 V ± 5%
Clock frequency range	15.2 ~ 27.2 MHz
Allowable input amplitude	1.28 Vp-p max

Table 1 Physical characteristics and operating conditions

Item		Typical value	
Power supply current	9 V	7	mA
	5 V	20	mA
Insertion gain		0	dB
Frequency response		-1	dB
Differential gain		3	%
Differential phase		3	deg
Noise		55	dB
Aliasing noise		50	dB
Insertion gain difference		3	%
DC output voltage difference		0.1	V

Table 2 Electrical characteristics

2-2. Electrical characteristics

The electrical characteristics of the IC are shown in Table 2. The power supply currents of 9 V and 5 V power supplies are 7 mA and 20 mA as typical values respectively. So, the total power dissipation of this IC is as low as 160 mW. The typical insertion

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gain is 0 dB. The frequency response is -1 dB at the point of 3.58 MHz compared with 250 KHz for signal frequency, when the clock frequency is fixed at 21.4 MHz. The typical differential gain is 3 %. The typical differential phase is 3 degree.

Two kinds of noise are defined. One is video noise in general use, and the other is so called aliasing noise. The typical signal to noise ratio is 55 dB, and the typical signal to aliasing noise ratio is 50 dB. The criterion of the signal to noise ratio is that the input signal amplitude is 1 Vp-p and the unit of noise is Vrms. The explanation of aliasing noise is shown in Fig.1. The aliasing noise occurs, if the gains of two CCD's for demultiplex mode are not equal exactly each other or the phases of two pulses for demultiplex mode are not shifted exactly 180 degree each other. The value of aliasing noise in Table 2 represents the difference between the amplitude of 3.58 MHz and 4.43 MHz spectra of output signal, providing that the input clock frequency is 16.02 MHz and the input signal frequency is 3.58 MHz. The 4.43 MHz spectrum is the sideband of one half of the input clock frequency of 8.01 MHz.

The typical insertion gain difference is 3 %. The insertion gain

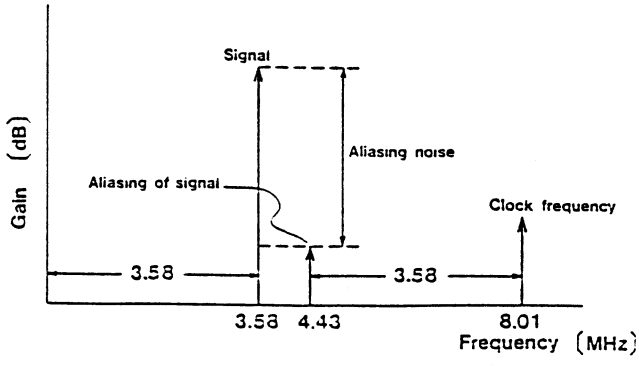

Fig.1 Aliasing noise

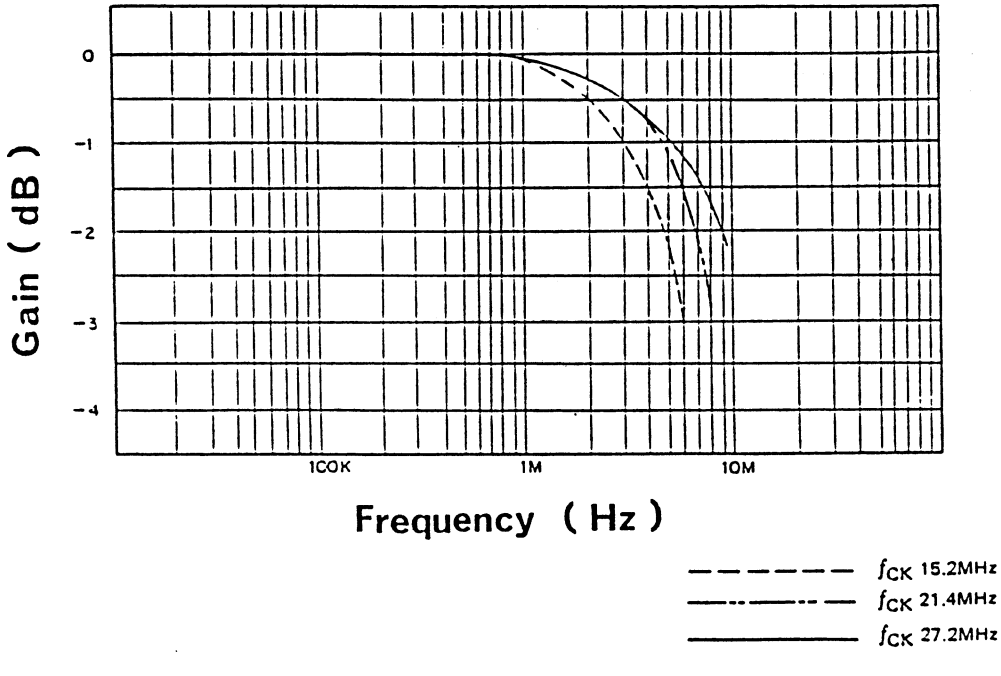

Fig.2 Frequency response

difference represents the change of insertion gain by changing the clock frequency. The typical DC output voltage difference is 0.1 V. The DC output voltage difference represents the change of DC output voltage by changing the clock frequency similar to the insertion gain difference.

The frequency response of the IC is shown in Fig.2. The horizontal axis indicates the input signal frequency. The parameter is the clock frequency. The higher the clock frequency, the better the frequency response for the signal, because the IC is a sampling system and the transfer function of the sample-and-hold circuit is changed by the clock frequency. The frequency response is as good as -0.6 dB at the point of 3.58 MHz, when the clock frequency is fixed at 27.2 MHz.

The relation between the clock frequency and the delay time of the IC is shown in Fig.3. Since this characteristic is nonlinear, this figure is used to find the clock frequency corresponding to the delay time for user's application. For instance, when the delay time is 70 μ sec, the clock frequency is 19.4 MHz.

3. Device structure

3-1. Fundamental structure

The block diagram of the IC is shown in Fig.4. Two CCD delay lines are used in demultiplex mode in order to decrease the power dissipation and to get better transfer efficiency. This IC contains a T-type flip flop, timing generators, clock drivers, autobias circuits and sync tip clamping circuits for input signal, and sample-and-hold circuits for output signal as peripheral circuits.

3-2. CCD structure

Each CCD delay line has 680 bits, so the CCD delay line of this IC is constructed of 1,360 bits. Consequently, the actual clock frequency of each CCD delay line is from 7.6 MHz to 13.6 MHz, though the input clock frequency is from 15.2 MHz to 27.2 MHz. The CCD for

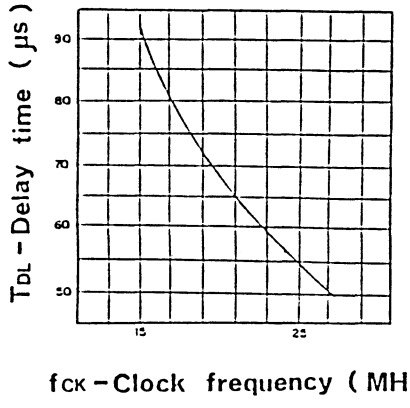

Fig.3 Delay time vs. Clock frequency

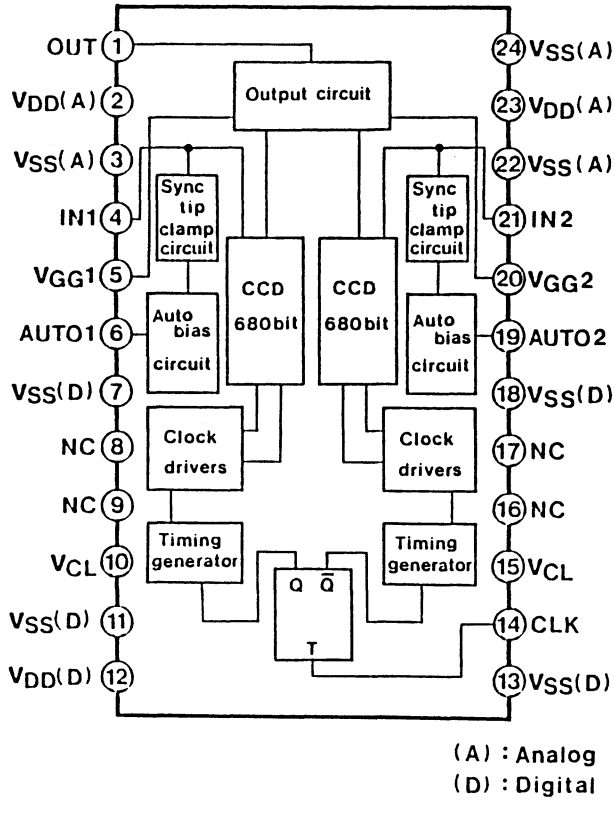

Fig.4 Block diagram of the chip

TBC is constructed by two layer polysilicon gates. The length per bit is 24 μm. The transfer clock pulses are two phases. The amplitude of the clock pulse is 5 Vp-p. The diode cut off method is adopted for the input of CCD. The signal charge of the CCD is transformed to signal voltage at the floating diffusion.

3-3. T-type flip flop

The T-type flip flop produces two clock pulses whose frequencies are one half of that of the input clock pulse. The phases of these two pulses are shifted exactly 180 degree each other. These two pulses are used for making several pulses for demultiplex CCD's, the autobias circuit and the output circuit.

3-4. Timing generator and clock driver

The timing generator generates several pulses from output pulses of the T-type flip flop. Those pulses are used for clock drivers of CCD, input gate pulses of CCD, precharge gate pulses of CCD and sample-and-hold pulses of the output circuit.

The clock driver is an inverter type made of N-channel and P-channel transistors.

3-5. Output circuit

The output circuit plays part in multiplexer, sample-and-hold, and output buffer. The output circuit is shown in Fig.5. The output circuit makes use of analog CMOS circuits. The two CCD's for TBC have the same output circuits each other before the each signal is multiplexed. The each output circuit of two CCD's for TBC has two sample-and-hold circuits. The output signals of two CCD's for TBC are multiplexed at the output node of the second sample-and-hold circuit. The sample-and-hold pulse amplitude of the first sample-and-hold circuit is 9 Vp-p, and that of the second sample-and-hold circuit is 5 Vp-p. The phases of the second sample-and-hold pulses are shifted 180 degree compared with the phases of the first sample-and-hold pulses. As its results, the coupling amount to signal with sample-and-hold pulses and the transient wave form are reduced. The output circuit consists of

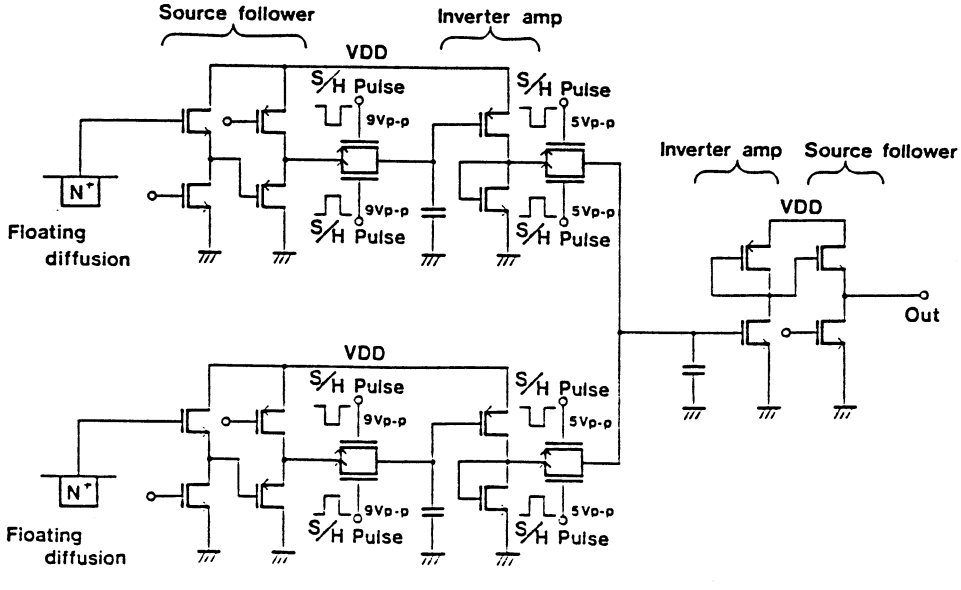

Fig.5 Output circuit

source followers and inverters. The inverters are adopted as a DC level shifter or an amplifier. The output buffer of this output circuit is made of source follower.

3-6. Autobias circuit and sync tip clamping circuit

The input bias of the CCD is adjusted at the most suitable level by the autobias circuit for input signal. The sync tip of input video signal is clamped to that autobias level by the sync tip clamping circuit.

The block diagram of the autobias circuit and the sync tip clamping circuit is shown in Fig.6. The autobias circuit for input signal has two CCD's. Both of them have the same structure as the CCD for TBC and only several charge transfer stages, but one of them is designed to have 20 % less maximum charge handling capability than the CCD for TBC. Comparing the outputs of two CCD's by an OP amplifier, the input signal bias is adjusted so that the charge of input signal is 80 % of maximum charge handling capability in the CCD for TBC. The sync tip clamping circuit consists of an OP amplifier and a diode. This circuit clamps the sync tip of input video signal to the adjusted level by the autobias circuit.

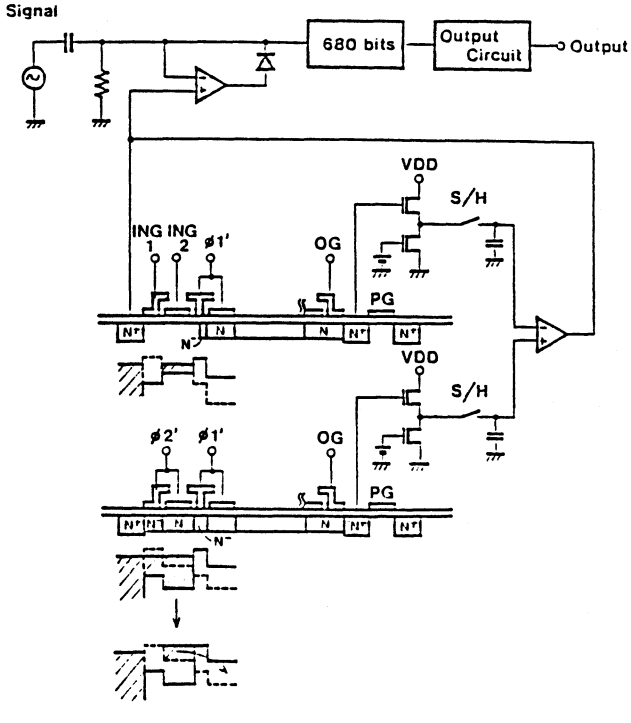

Fig.6 Block diagram of the autobias circuit and the sync tip clamp circuit

3-7. Wafer process

The cross section of the IC is shown in Fig.7. The substrate is P type. The N-well is constructed for P-channel transistor. The N-channel transistor is constructed on the substrate. The field oxide is constructed by LOCOS method. The channel stop of the N-channel transistor and the CCD is made from ion implantation of boron. The minimum polysilicon gate length of the transistors is 4 μm. The gate oxide thickness is 500Å. The gate insulator of the CCD is made of SiO2-SiN-SiO2. The CCD for TBC is buried channel type except the input part.

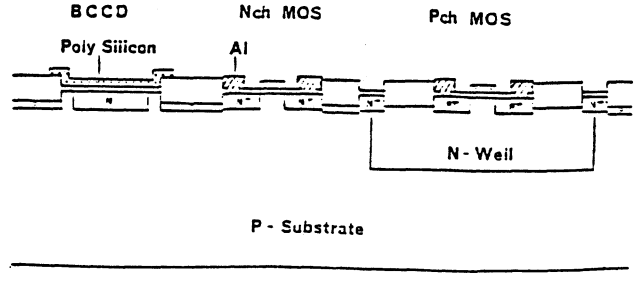

Fig.7 Cross section of CMOS-CCD

4. The external circuits

The external circuits for application is shown in Fig.8. Only one capacitor and one resistor are sufficient as the external circuit for signal input. The capacitor is utilized for AC couple of signal input. The resistor is utilized for input bias current of CCD for TBC. The two signal input terminals of this IC may be connected with each other. An emitter follower using PNP transistor is recommemded to connect the output signal terminal of the IC. The low pass filter is necessary as a harmonic suppresser filter. The VGG1 and the VGG2 terminals of the IC may be connected with each other. The bias of these VGG terminals needs to be adjusted by an external variable resistor so that the sync tip level of the output video signal may be 2.7 V. The clock pulse input terminal needs one capacitor and two resistors. The capacitor is utilized for AC couple of clock input. The resistors are utilized for input bias circuit of the terminal. The AUTO1 and AUTO2 terminals are connected to decoupling capacitors in order to prevent oscillation.

The recommended wave form of the input clock pulse is shown in Fig.9. 2 Vp-p is sufficient for the amplitude of the input clock pulse. The low level of the input clock may be from 0 V to 1 V,

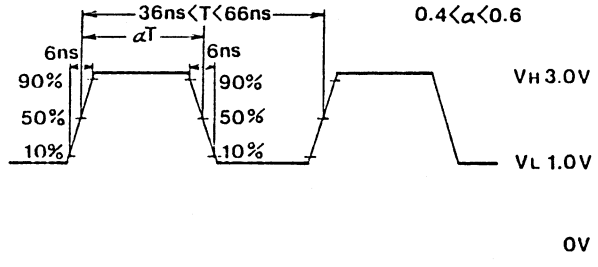

Fig.9 The input clock pulse waveform

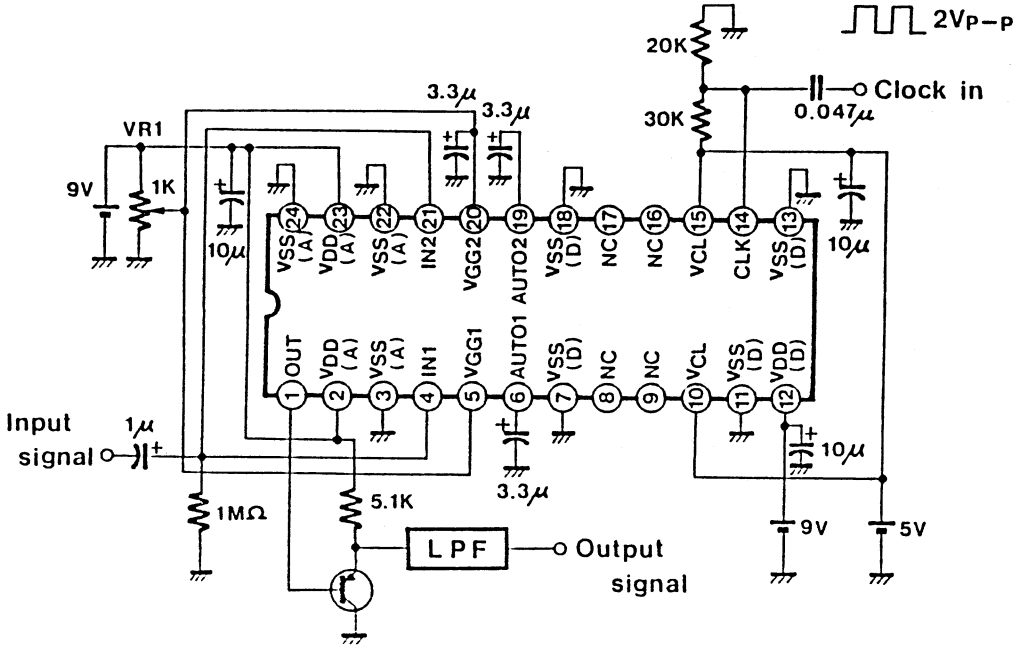

Fig.8 External circuit for application

1. Wide delay time range by high clock frequency (50 μ sec ~ 90 μ sec)
2. Demultiplex CCD for low power dissipation and better transfer efficiency
3. T-type flip flop for low aliasing noise
4. Output circuit with multiplexer
5. CMOS-CCD Process for low power dissipation of 160 m W.

Table 3 Features of the IC

and the high level of that may be from 3 V to 5 V. The rise time and the fall time are 6 nsec. One period time is changeable from 36 nsec to 66 nsec. The ratio of the pulse width to one period may be from 0.4 to 0.6.

5. Conclusions

We developed a CMOS-CCD signal processor for video signal TBC. The features of the IC is shown in Table 3. First, the IC has the wide delay time range from 50 μsec to 90 μsec by using high clock frequency. Second, the IC is adopted the demultiplex CCD's in order to get low power dissipation and better transfer efficiency. Third, the T-type flip flop is integrated in order to suppress the aliasing noise. Fourth, the output circuit with multiplexer is integrated on the chip. Fifth, the IC is manufactured by CMOS-CCD process for low power dissipation of 160 mW.

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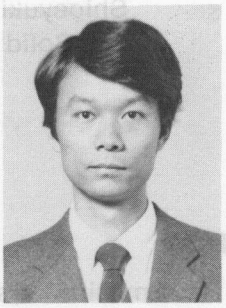
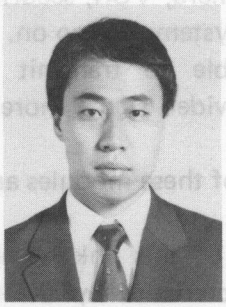
Biographies

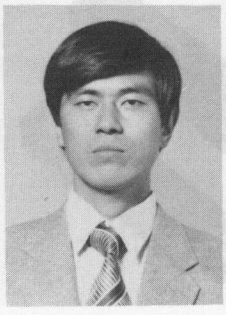


Tadakuni Narabu was born in Tochigi, on May 30th, 1955. He received the B.S. degree in Electronic Engineering from Tohoku University in 1978. He joined Sony Corporation Research Center, Yokohama, in 1978, and engaged in research and development of CCD. Presently, he engages in research and development of CCD and MOS LSI for video signal processing in Semiconductor Group at Atsugi Plant.

Miaki Nakashio received her B.S. degree in Instrument Engineering in 1979 from Keio University, Kanagawa, Japan. She joined Sony Corporation, Semiconductor Division in 1979. She worked on development and design of signal processing CCD from 1979 to 1985. At present she works at Video Products Division No.1, Communication Products Group.



Fujio Shimura received his B.S. degree in Electrical Engineering in 1984 from Tokyo Electrical Engineering College, Tokyo. He joined Sony Corporation, Video Products Division No.1 in 1984, where he worked on development and design of signal processing CCD for Video Disc Player from 1984 to 1985. At present he works at Video Products Division No.1, Communication Products Group.



Katsuyuki Saitoh was born in Miyagi, Japan, in 1956. In 1975 he joined the Sony Corporation as a member of the Process Engineering Staff of the Production Department of the Semiconductor Group. From 1981 to 1985, he worked on development and preproduction of MOS LSI and CCD. At present, he has been working on Application Engineering Department of the Semiconductor Group.