THAM 19.3

A NEW DIGITAL VIDEO SIGNAL PROCESSING SYSTEM FOR A VIDEO DISC PLAYER

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ABSTRACT

We have developed a new digital signal processing system for a video disc player, based on a feed forward technique. This report describes the newly developed system.

The system is composed of two LSI units: a signal processing LSI for the TBC (time base error corrector), which constitutes the basic block incorporating A/D and D/A converters; and an LSI for additional functions including the FNR (field noise reducer).

INTRODUCTION

Improved picture quality, cost reduction and extensibility are required in video signal processing for video discs.

To meet these requirements, we have developed a new video signal processing system which uses digital technology to improve picture quality. It is highly extensible in that the basic block can be developed to provide additional functions.

The entire system can be constructed of two LSI units.

The features of the system are as follows.

1. A basic block that utilizing only an LSI for digital TBC containing A/D and D/A converters;
2. A new feed forward velocity error corrector adaptable for still pictures and FNR;
3. An FNR that shares memory with a field synchronizer and is capable of processing composite signals; and
4. A linear phase digital noise canceler with high waveform reproducibility.

SYSTEM CONSTRUCTION

Fig. 1 shows the block diagram of the entire system. The system is composed of two C-MOS LSI units. The master clock frequency is 4 Fsc (14.31818 MHZ). The video signal is quantized into eight bits.

The basic block is realized by an LSI for digital TBC having A/D and D/A converters. An FM signal detected by the pickup is demodulated, and input to the built-in 8-bit A/D converter. After drop out compensation, the input signal is written in the FIFO (first input first output) memory in response to a clock pulse which follows the jitter of the input video signal. The clock pulse is generated by the built-in digital PLL (phase-locked-loop) circuit. The high-frequency jitter cannot be removed from the input signal when the signal is written in the FIFO memory. To remove the residual jitter, reading clock generated by the digital VCO is phase-modulated according to the residual jitter so that jitter can be removed at high accuracy when the video signal is read.

The system uses the velocity error correction method to eliminate residual jitter in a 1H (1 horizontal synchronous) piriod. This method obtains jitter error through the linear interpolation. In the last stage, the system reduces disc noise and mixed modulation noise of FM audio signal in the video signal by the noise canceler circuit, and outputs the video signal from the built-in 8-bit D/A converter.

The extension block of the system receives 8-bit digital data output from the basic block. As a field synchronizer, the extension block allows a special reproduction function for still pictures and searching, using a field memory of 2M-bit. Simultaneously, the block uses an FNR to improve the S/N of the video signal. Following that, a three-line logical comb filter separates the video signal into luminance and chrominance signals,and these separeted signals are output from the respective D/A converters. When luminace and chrominance signals are output from the D/A converters, the clock is phase-modulated in accordance with the residual jitter by the clock modulation circuit of the basic block, so that the jitter is removed effectively from the video signal.

NEW FEED FORWARD TIME BASE ERROR CORRECTOR

Conventional velocity error correction has the problem that application is restricted to the basic block of the system. Consequently, when there is a field memory in the upstream of the D/A converter, obtainingit residual jitter information on which the clock modulation for D/A conversion is based is not possible. Therefore, velocity error correction cannot be performed, or a residual jitter detection circuit needs to be provided immediately before the D/A converter.

To solve this problem, the new system employs a new velocity error correction method. Specifically, time base error

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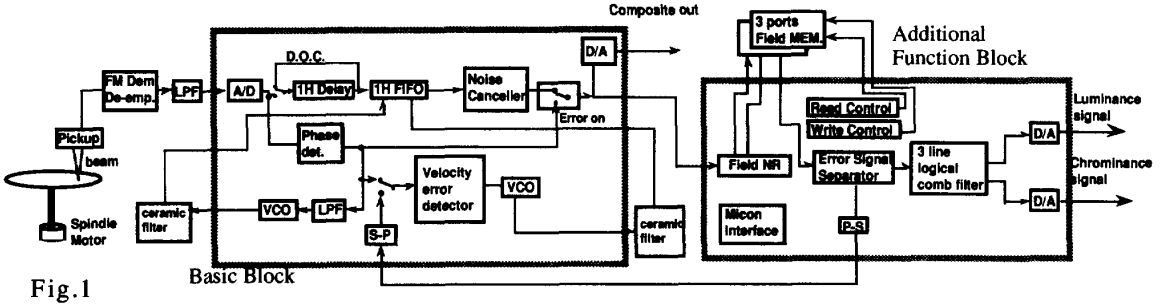

Fig.1

information is superimposed on the horizontal synchronization signal of the video signal as shown in Fig. 2. This error information is sampled from the video data read from the memory, and is fed back in form of serial data to the basic block, by the circuit construction shown in Fig. 3. On the basis of this data, the clock is phase-modulated in the basic block.

With this method, velocity error correction is possible even for a video signal output from a synchronizer using a memory. In addition, when FNR is operated, it can process video signal and error information simultaneously for field noise reduction. Since the processed error information always corresponds to the processed video signal, hue noise can be reduced substantially . Thus, this method niether restrict the circuit construction nor require any additional circuit before the D/A converter, and enables the system to conduct velocity error correction if it performs computation for FNR or other functions.

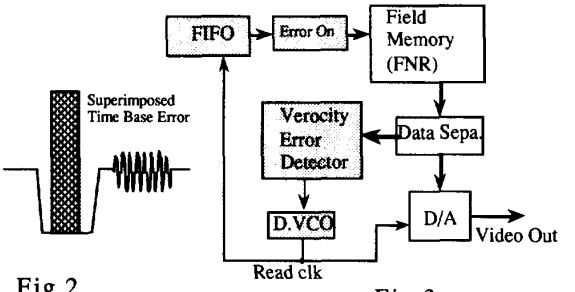

Fig.2

Fig.3

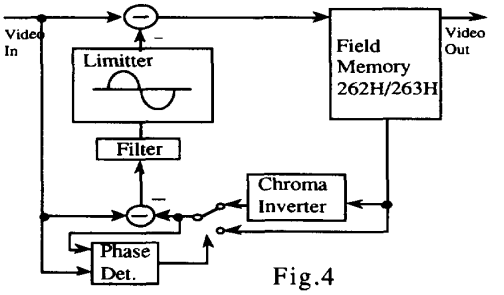

Fig.4

FIELD NOISE REDUCER

The new system uses the field memory of a synchronizer to constitute a feedback FNR (field noise reducer).

This FNR is capable of processing composite signals, and is adaptable to the phase modulation method employed for the reading clocks (described previously at the velocity error correction section). Due to these advantages, the FNR provides an efficient circuit construction permitting smooth selection of a still picture and substantial noise reduction.

Fig. 4 shows the circuit construction of the FNR. Using the three-port memory, the FNR selects either 262H or 263H, for each field, for the delay of a video signal to be fed back. And the FNR passes the video signal through the chroma inverter only when the delay is 263H. It reduces the noise in composite video signals effectively, utilizing the correlation between fields. The feedback coefficient is adaptive according to the correlation with the video signal. Furthermore, the feedback coefficient for the superimposed time base error is independent of the video signal, which helps to improve the S/N effectively in particular.

DIGITAL NOISE CANCELER

In addition to the FNR described above, the new system has a digital noise canceler circuit in the basic block to minimize noises of a video signal. This circuit is able to reduce noises of a video signal with a high waveform reproducibility and without causing signal distortion and ringing that occur in conventional analog circuits. In addition, the number of components used in the circuit is decreased substantially due to the LSI construction.

CONCLUSION

A highly efficient one-chip TBC has been realized by using an effective LSI layout with built-in high-speed A/D and D/A converters.

Furthermore, a highly extensible, high function and high performance digital signal processing system has been realized to improve picture quality substantially and permits velocity error correction even when an additional function is operated.